340 GHz Frequency Multiplier with Unbalance Circuit Based on One Schottky Diodes Chip

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Abstract— **This Terahertz is a new across research field. This paper introduces a design of multiplier at 340 GHz with discrete GaAs planar Schottky diode. The 50um thick quartz circuit substrate is flip-chip mounted for diode thermal dissipation. A proposed Schottky diode model improves the accuracy of design which is considered behaviours of current voltage (I/V) and capacitance voltage (C/V), plasma resonance and skin effect. Diode embedding impedances were calculated by full-wave analysis and harmonic-balance (HB) simulation tools with an coaxial port to represent the nonlinear junction for circuit matching. In the circuit, one stage Compact Suspended Microstrip Resonators (CSMRs) are used for low-pass filter (LPF) at input port and a hammer-head filter is used for DC port. Two low-pass filters minimize the length/width ratio. The doubler is self-biasing and fix-tuned, the highest efficiency is 5.1% and output power is 1.1 mW @ 329.6 GHz with input power 20mW.**

INTRODUCTION

Frequency multipliers based on Schottky barrier diodes play a crucial role at frequencies ranging from 300 GHz to 3 THz. Over the years, these devices have remained critical to a variety of submillimeter-wave heterodyne-based instruments [1] including radiometers for space-borne applications, receivers for ground-based radio astronomy, and sources for vector network analyser frequency extenders. Planar Schottky technology made tremendous progress in the late 1990s, principally thanks to the astrophysics community that supported the construction of the heterodyne instrument on Herschel [2] [3]. Because of low output power of semiconductor three ports device, GaAs planar Schottky diode technology plays a crucial role in THz and sub-THz regions in two decades. Frequency multipliers based on Schottky diode are nonlinear devices that generate harmonics of an input sine signal. Through matching networks at the input and output frequencies, optimize the transfer of power from the fundamental frequency to the desired harmonic and get the wanted harmonic and suppress undesired ones, Fig. 1 shows the schematic diagram of the multiplier. Because the balanced multiplier has a high output power and efficiency, it becomes the popularity topology for frequency multiplication.

However, due to the limit of planar Schottky Diode and membrane technics, most of multiplier had a low frequency and output power: the frequency is less than 400 GHz [4] and the max output power is up to 20mW at 170GHz which is failing to drive a 340GHz balanced doubler. This paper focuses on 340GHz frequency multiplier including waveguide block, quartz and one Schottky Diodes Chip with three anodes in series.

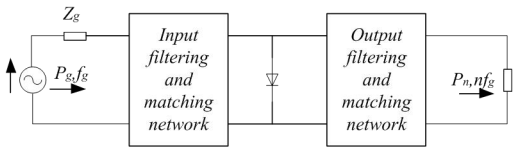

Fig. 1 The Schottky diode multiplier schematic diagram

DESIGN

The structure diagram of the 340GHz frequency multiplier is shown in **Fig. 2**. The quart circuit extend from the bias voltage port, input waveguide (WR5) to output port WR2.8. There are two low pass CSMRs (Compact Suspendered Microstrip Resonators) filter in the circuit beside input port respectively. The Schottky Diodes Chip placed between ground and Suspendered Microstrip.

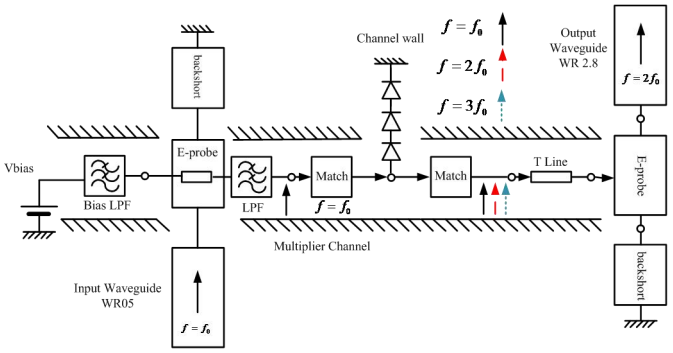

Fig. 2 Structure diagram of the 340GHz frequency doubler

Schottky diode model: Schottky Diodes Chip with three anodes in series is used in this doubler. The Schottky diode model includes two parts: diode spice model in ADS (Harmonic Simulation Software) and 3D structure model in HFSS (3D electromagnetic simulation software). The spice model can be got from I-V and C-V curves [5]. Each anode has a series resistance of 3 ohm, ideal factor 1.25, Junction

capitation Cj(0) is 30fF, forward voltage is 0.65V and Cpar is about 6fF.

Circuit simulation: combine harmonic simulation software with 3D electromagnetic simulation software, an optimum result can be got. When the bias voltage is -3V and input power is 13dBm, impedances at input and output are Z_LO=7+12i, Z_RF=81+162i. Finally, the simulation result is shown in Fig. 3. The simulation includes five parts: input probe, output probe, Diode placement, improved CSMRs filters and match networks.

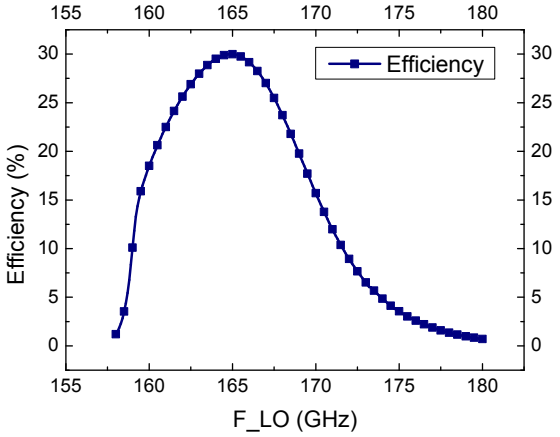

Fig. 3 Simulation results with ADS and HFSS, shows the efficiency vs drive frequency

In the quartz circuit, the CSMRs lowpass filter have a great performance with a passband from DC to 200GHz and stopband from 270GHz to more than 450GHz. The structure and simulation results of CSMRs filter between input waveguide and Schottky Diodes Chip are shown in Fig. 4.

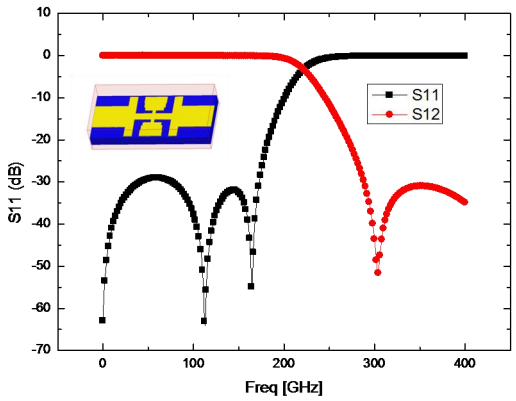

Fig. 4 simulation results and structure of CSMRs filter

Architecture And Measurements

The fabricated 340GHz frequency doubler is shown in Fig. 5. The multiplier is made up a waveguide block split in the E-plane. The planar diodes are flipped-chip mounted between a 50um quartz-based microstrip circuits and metal channel wall.

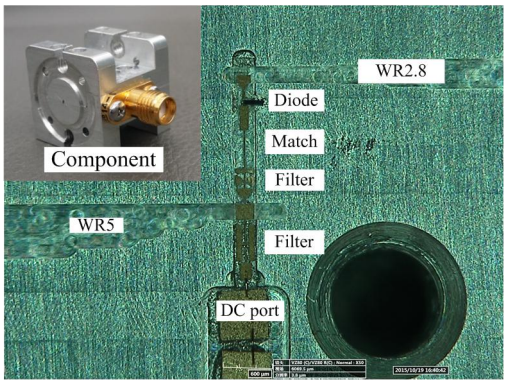

Fig. 5 Photograph and detail of 340GHz multiplier

For the measurements, a commercial signal generator was used to driver an MMIC based quadrupler with max output power of 40mW at 80GHz~86GHz [6], and all the measurements were done at room temperature. W-band amplifier has a power of 110mW to drive a 170GHz multiplier with 20mW output power. 340GHz multiplier was driven by 170GHz multiplier and detected by PM4 (Power Meter 4). The testing platform is shown in Fig. 6.

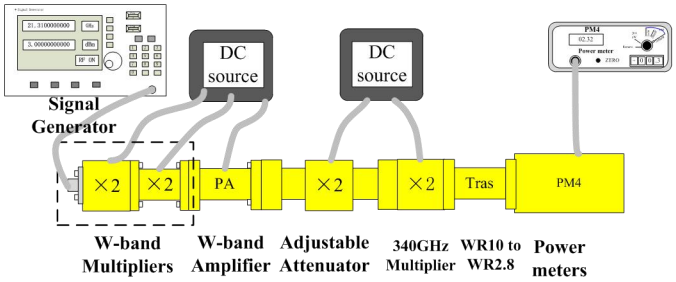

Fig. 6 340GHz multiplier testing platform

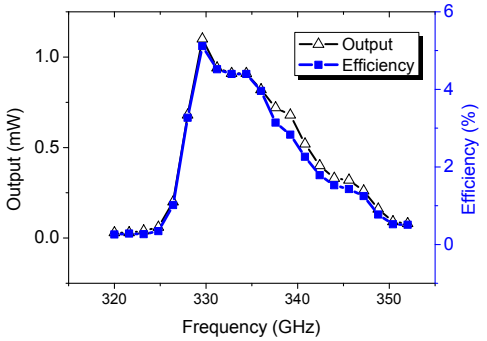

Fig. 7 340GHz multiplier output power and efficiency vs output frequency.

Conclusions

This paper focused on design and measurements of 340GHz multiplier. It presented one kind of unbalance multiplier structure based on one Schottky Diodes Chip and improved CSMRs filter. CSMRs filter can reduce the ratio of length/width and it is useful for fabrication. That one Chip used in this component reduced the cost of multiplier and it is suitable for low power driver. The details of measurements have been shown in Fig. 7. The highest efficiency is 5.1% and output power is 1.1 mW @ 329.6 GHz with input power

20mW. The typical tested power is 3% and output power above 0.5mW in 328GHz ~ 340.4GHz.

ACKNOWLEDGMENT

This work was supported by Institute of Electronic Engineering, Microsystem and Terahertz Research Center, China Academy of Engineering Physics (CAEP-IEE) and National Key Basic Research Program of China (973 Program) with Grant No.2015CB755406.

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