A 1.5 W 3 GHz Back-End Processor in 65-nm CMOS for Sub-millimeter-wave Heterodyne Receiver Arrays

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Abstract—As compact sub-millimeter wave heterodyne receiver technology continues mature rapidly, astronomers have begun to implement array-based instruments with full receiver arrays up to 64 pixels already demonstrated. While this impressive technology solves many of the key problems related to heterodyne arrays (LO generation and distribution between pixels, antenna array fabrication with well controlled beam patterns, and IF chains with low inter-pixel crosstalk), one challenge that remains in these and even larger arrays is that of back-end processing implementation. While several FPGA-based spectrometer processors exist, these systems consume power on the order of 30-50 W making their accommodation a challenge when a large number of pixels is required, as the back-end power is inflated by the number of pixels.

CMOS system-on-chip (SoC) technology is the advanced electronics technology used in mobile electronics such as smartphones/laptop, and provides an avenue to address this back-end power challenge head on. Several studies describe how a dedicated CMOS SoC offers 10-100X less power consumption compared to an FPGA implementation performing the same digital operation. This is primarily as a CMOS SoC is not required to carry the additional circuitry required to support re-configurability, greatly reducing the capacitance, and in turn, power consumption per logic cell. Additionally, CMOS SoCs allow for not only digital, but also analog and mixed-signal circuitry to be co-integrated within a single chip solution, enabling a drastic reduction of power consumption related to interfaces as the large capacitances of off-chip PCB traces and device packages no longer have to be driven with high-speed digital signals. This because an SoC-based spectrometer allows the digitizer can be integrated directly with the digital processing core into a single chip.

This work presents a fully integrated 3 GHz bandwidth (6 GS/s) back-end processor, which is implemented in advanced 65-nm CMOS process, for sub-millimeter heterodyne spectroscopic instrumentation. The spectrometer processor contains a 3-bit/interleaved-by-2 flash analog-to-digital converter (ADC), a 4196-point fast Fourier transform (FFT) processor, and a 4-billion-count data accumulator (ACC). For accurate digital timing, the chip contains an internal programmable frequency synthesizer providing a timing-skew controlled clock to each system block. In order to overcome process/temperature variations, a replica ADC is designed, offering key-components' bias-conditions. Additionally, integrated resistor-based 8-bit digital-to-analog converter (DAC) provides programmable reference levels to the ADC, reducing constant DC power and offering ways to calibrate mismatch issues between interleaved ADC channels. The chip consumes a total of 1.5 W and is embedded within a compact PCB module and a USB connection for data readout and configuration of chip settings.