All-NbN Technology on Sapphire Substrates for SIS-based THz Receivers

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***Abstract*—Heterodyne SIS receivers for THz radiation have been investigated and successfully employed in the past. In order to push the operation frequency beyond the 700 GHz limit, superconductors other than Niobium (Nb) have to be used. We have developed a NbN/AlN/NbN technology for the fabrication of high-quality SIS junctions on sapphire substrates. The main optimization criteria are the energy gap of the superconductor along with the leakage current and the critical current density. The development of our technology resulted in gap voltages as high as 5.1 mV with critical current densities and leakage currents that are suitable for the realization of SIS mixers. Based on the material parameters that have been extracted from our technology, we have developed an RF design of a prototype for an integrated receiver using the all-NbN fabrication process. We have demonstrated transmission of 600 GHz radiation generated by a flux-flow oscillator to an SIS mixer integrated on the same chip.**

I. Introduction

Heterodyne detection of terahertz signals using Superconductor Insulator Superconductor (SIS) mixers has shown to be capable of quantum limited detection while simultaneously enabling high resolution spectroscopy [1-4]. This quantum limited operation is possible up to an upper frequency limit which is given by the energy gap of the superconducting materials used for the electrodes of the SIS devices and the RF circuits. The most popular material in the past decades has been pure Niobium (Nb) which can be operated up to 700 GHz. In order to push this limit to higher frequencies, other superconductors have to be used, such as Niobium nitride (NbN) or Niobium titanium nitride (NbTiN). These materials can exhibit twice the energy gap of pure Nb thus enabling the low loss operation up to 1.4 THz.

However, realizing these materials with the required high quality is much more challenging as compared to pure Nb. NbN based technology has been demonstrated already, achieving the highest energy gap of up to 6 mV on Magnesium oxide (MgO) substrates with high critical current densities up to 70 kA/cm² [5]. Other groups have demonstrated a high-quality NbN technology on sapphire or silicon substrates where, either a buffer layer had to be used or an elaborate pre-treatment of the substrate is necessary [6,7]. In order to decrease the complexity of the fabrication process, we aim at the realization of all-NbN technology directly on R-plane sapphire substrates.

Apart from the energy gap of the superconductor, there are several other requirements to the trilayer properties in order to be suitable for a low noise receiver operation, such as the leakage current through the barrier and the critical current density j_c. These two parameters, however, are not uncorrelated, but defined by the barrier itself and the interface between the barrier and the electrodes. Thus, the surface of the NbN base electrode has to be ultimately smooth in order to realize a proper barrier.

Not only the leakage is affected by the critical current density, but also the specific capacitance C' of the trilayer increases with higher j_c values. Therefore the fabrication process needs to allow for the realization of sub-µm sized mixers.

We have developed a trilayer deposition process for high gap voltages along with adequate leakage and critical current densities. In order to achieve a process allowing for the fabrication of high-quality SIS devices as well as proper RF circuits, the fabrication has been optimized considering the various requirements. The quality of the SIS trilayers is evaluated using the Josephson junction (JJ) quality parameters at an operation temperature of 4.2 K.

II. Technology Development

The development of the deposition process for high-quality SIS devices requires a careful optimization of each layer involved, as well as a close process control. We have developed a 3-chamber DC magnetron sputtering system, with a movable heater stage, enabling the in-situ deposition of the trilayers at 775 °C. The main optimization criteria are the energy gap of the superconductor ($\Delta=V_{gap}/e$), the leakages through the barrier and the critical current density j_c. As already reported in [8], the gap voltage was optimized to values up to 5.1 mV, allowing for operation frequencies above 1 THz. A measure for the leakage currents, the subgap ratio, is derived from the resistance in the retrapping branch at 3.5 mV (R_{sg}) normalized to the normal state conductance R_N, which is obtained by a linear fit in the normal state regime. Figure 1 shows the measured values over a wide range of critical-current densities. The subgap ratio clearly decreases towards higher j_c values due to the decreasing thickness of the barrier. As expected, the gap voltage (≈ 5 mV) in turn does not depend

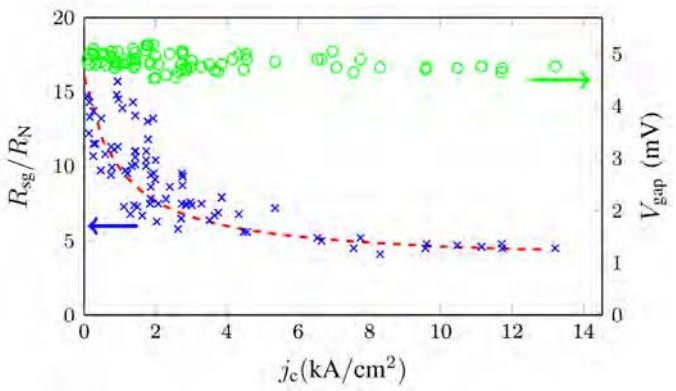

Figure 1: Dependence of the subgap ratio (R_{sg}/R_N, ×) and the gap voltage (V_{gap}, ○) on the critical-current density j_c. The dashed red line is to guide the eye.

on j_c, but shows some fluctuations about 10 %. In our opinion, this is due to minor flucutiations of the deposition parameters which, in the current setup, cannot be avoided without some modifications to the deposition system. Nevertheless, the achieved quality of the trilayers seems suitable for the realization of an SIS receiver.

In order to fabricate high frequency devices, not only the trilayer quality, but also the peripheric materials and the patterning of each layer is of utmost importance. The fabrication process as described in detail in [9] and [10] is used, but it has required modifications mainly concerning the thickness of the different layers. The thickness of the electrodes is selected according to the London penetration depth of NbN ($\lambda_L \approx 200$ nm). The minimum realizable mixer size with this fabrication process is about $A_{mix} = 500 \times 500$ nm². The fabrication process must also accommodate the realization of a microstrip waveguide with an appropriate characteristic impedance range. The waveguide is formed by the base electrode of the trilayer as ground plane, the dielectric formed by the insulating layer (SiO) and the wiring layer creating the microstrip itself. Therefore, the thickness of the isolator in conjunction with the feature sizes of the wiring layer defines the characteristic impedance of the microstrip. The thickness of both, the insulator, as well as the wiring layer was selected to $d_{SiO} = d_{wiring} = 400$ nm. Optimization of the patterning resulted in minimum feature sizes in the wiring layer of 700 nm. The achievable characteristic frequency thus ranges from ≈70 Ω to less than 10 Ω, which is suitable for the impedance matching that is required on chip.

Apart from the geometrical properties of the wiring layer, also the superconducting properties are important. Since the wiring layer defines the microstrip line, it has to allow the THz radiation to travel from e.g. the antenna to the mixer. Therefore, the energy gap needs to be large enough, analogue to the mixer electrodes. The optimization of superconducting properties of the wiring layer led to a transition temperature of $T_c = 14$ K which is more than 1 K lower than the transition temperature of the electrode material. This results from the fact that the wiring layer is made in the very last fabrication step, and therefore, has to be deposited at room temperature as opposed to the electrode material. In addition to that, the wiring layer does not have the bare, clean substrate

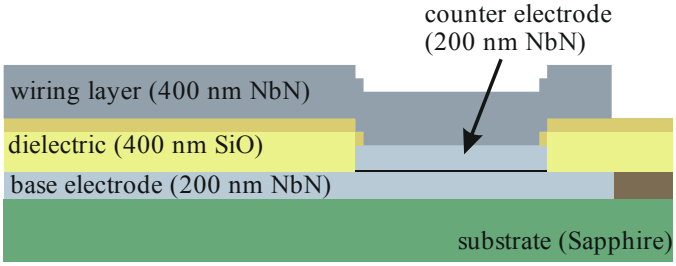

Figure 2: Schematic cross-section of the modified fabrication structure.

underneath, but it has to be deposited on top of various materials, namely the NbN of the counter electrode as well as amorphous SiO. This is why the wiring layer cannot reach the quality level of the electrode material. In the future, the wiring layer material might be replaced by NbTiN which can be deposited with high quality even on amorphous substrates [11], [12], thus allowing for low loss transmission lines on chip for ultimately high operation frequencies.

III. RF Prototyping

Considering the obtained material parameters of each single layer, RF simulations can be performed. The simulations were conducted using CST – Microwave Studio. The actual material parameters were included in the simulation. The superconductor parasitics were derived from the Mattis-Bardeen theory from DC measurements. The intrinsic mixer capacitance was obtained using the designed mixer area and the specific capacitance C' of that trilayer, which in turn was calculated by the relation between C' and the critical current density which in this case was 6 kA/cm².

The first prototype was designed comprising a flux-flow oscillator (FFO) and an SIS mixer along with an appropriate RF circuit that connects both of these devices. This RF circuit has to fulfill a number of requirements including the impedance matching of the FFO to the mixer, thus providing a good RF transmission. This impedance matching does not only include the transformation of the real parts of the impedances into each other, but also the imaginary part of the mixer input impedance needs to vanish for the design frequency. This imaginary part arises from the intrinsic capacitance of the SIS mixer. A tuning structure is used to tune out this capacitive imaginary part of the impedance. Figure 3 depicts a scanning electron microscope (SEM) image of a realized prototype. The tuning structure and the SIS mixer are in the left part of the image as well as in the close up. In this case, this tuning structure is realized by a butterfly stub which is connected to the microstrip waveguide in a certain distance to the mixer l_{tune}.

While providing a good RF connection between FFO and mixer, the connection needs to be interrupted for DC, since both devices have different DC operation points. This is achieved by a DC break for each electrode which can be seen in the center of figure 3. The DC break design is similar to what can be found in [13], since these designs proved to exhibit excellent performance of both, transmission level and bandwidth. Yet, the designs had to be adapted to our technology.

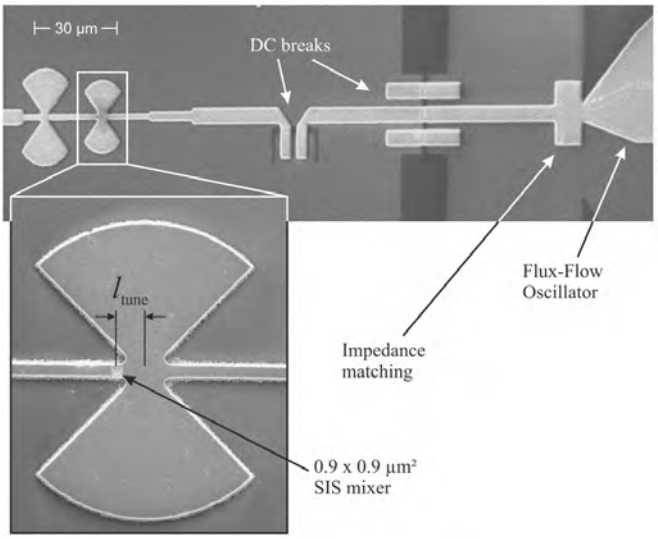

Figure 3: Scanning electron microscope image of an RF prototype comprising the FFO, the RF-circuit and the SIS mixer.

The fabricated prototypes were measured at 4.2 K immersed in a liquid helium transport dewar. Figure 4 depicts a current-voltage (IV) measurement of an, in this case, 0.9x0.9 µm² sized SIS mixer with (—) and without (—) FFO radiation. The gap voltage is at 4.5 mV with a critical-current density of 6 kA/cm² and a suitable subgap ratio of 8.

The RF design also incorporated a control line which is supposed to suppress the critical current of the mixer by magnetic field. However, the critical current of the control line was not high enough to fully suppress the critical current of the mixer. That is why the IV curve is shown here without magnetic field.

Applying FFO radiation induces Shapiro steps and photon assisted tunneling (PAT) steps in the IV curve (see —). The Shapiro steps are clearly visible up to the third order in the central part of the image. The photon assisted tunneling steps appear below as well as above the gap. Below the gap, Shapiro steps and PAT steps interfere, however, above the gap, this PAT step is clearly visible. This measurement is done at an FFO frequency of 540 GHz. Using the current in the retrapping branch at a certain voltage (e.g. 3 mV) as a measure of the RF power accepted by the mixer and conducting this measurement for many frequencies, allows to create a spectrum of transmitted power. This can be compared to the RF simulations done for that particular design as it is shown in the inset of figure 4. Except for the bandwidth, the simulation closely matches the measurement, not only the peak transmission frequency of 600 GHz, but also the shape of the frequency response is almost identical. We have successfully realized a number of designs with variable tuning length and different tuning structures on the prototype chip. The results thereof will be shown elsewhere.

CONCLUSIONS

The thorough fabrication-process development for SIS receivers based on NbN/AlN/NbN trilayer allows the realization of high quality sub-µm SIS mixers as well as microstrip waveguides with a large characteristic impedance range. Due to the optimization of the particular material

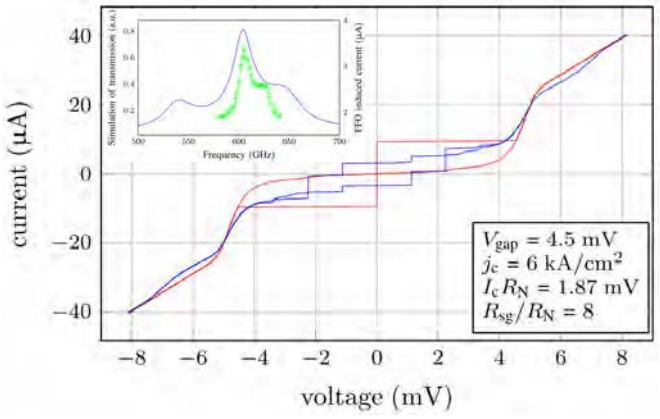

Figure 4: Current-voltage characteristic of a mixer with (—) and without (—) FFO-radiation. The inset shows the FFO induced current (—) versus frequency along with the simulated transmission (—).

properties, each layer should be able to carry frequencies higher than 1 THz. Furthermore, all material parasitics were studied, which is very important for the simulations of the RF circuit, in order to create a design for an SIS receiver.

The achieved gap voltages of 5.1 mV are suitable for operation frequencies above 1 THz. By extracting all necessary material parameters, RF simulations were conducted, resulting in a design of a prototype device, consisting of flux-flow oscillators integrated with SIS mixers on the same chip. The study of the frequency response of the realized structures proved a good agreement with the simulations even at frequencies as high as 600 GHz. In the future, we plan to incorporate an antenna in the design allowing the study of a fully integrated receiver.

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