A Novel Full Band Terahertz Frequency Quadrupler

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***Abstract*—This paper presents designs of a novel full band quadrupler based on GaAs membrane technology. The measured quadrupler output power is more than -28 dBm at the full WR-1.0 band, and the measured peak power achieves above -13 dBm at 950 GHz with 7 dBm driven power.**

***Index Terms*—quadrupler, membrane substract, Schottky diode, submillimeter wave, terahertz.**

I. Introduction

Terahertz sources have attracted recent interest for terahertz measurement and radio astronomy applications [1], [2]. For such applications, it is important to have compact sources that produce enough power and own broadband performance.

Solid-state devices provide a compact and robust solution for the generation of terahertz signal. Transistor with smaller feature size have been demonstrated with maximum frequencies of oscillation (fmax) above 1 THz and practical circuit operation has been extended into the lower end of the terahertz (THz) frequency band. Although rapid advances have been made in amplifiers[3], especially high electron-mobility transistor (HEMT) [4] and heterojunction bipolar transistor (HBT) [5], Schottky diodes still provide high performance cost ratio and are widely used in terahertz frequency multiplier sources [6],[7]. For terahertz multiplier sources, cascading multipliers is a pragmatic approach. It typically consists of a chain of doublers and triplers, selected to yield the desired output frequency with a efficiency[8],[9]. The final efficiency of a multi-stage chain, as a result, is often on the order of a few percent or less [10]. Moreover, interstage mismatches in the chain can readily influence adjacent stages by pulling them from their optimum operating status and reducing efficiencies. Direct multiplication to a high-order harmonic greater than the third is desirable for higher frequency band, even with the challenges including proper termination of all intermediate harmonics (idlers). Also, a high-order harmonic multiplier brings the improvement on size, weight, power, and cost (SWaP-C).

This work presented here applies the architecture to implement an integrated frequency quadrupler fabricated on GaAs membrane substrate. This Quadrupler features 2 anodes in series configuration monolithically is integrated on a GaAs membrane substrate and connected to a split waveguide-block by metallic beam-leads. As we know. It is the first quadrupler working at the full WR-1.0 Band.

II. Quadrupler Development

A. Circuit topology

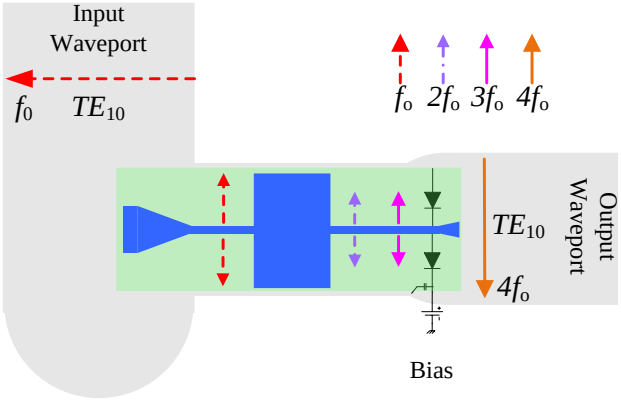

Fig.1. Block diagram of the balanced quadrupler.
f_o: the input fundamental frequency,
$2f_o$: the second idle harmonic frequency,
$3f_o$: the third idle harmonic frequency,
$4f_o$: the output fourth harmonic frequency.

Fig. 1 illustrates the basic architecture of the quadrupler circuit developed in this work. The diodes pair is placed in the output waveguide, and the two diode branches are antiparallel connected to the input fundamental signal on a TEM mode and series connected to the output 4th harmonic output signal on a TE mode. Usually, only even-order harmonics are generated due to the balanced configuration. Considering small asymmetries are introduced by the physical structure of the Schottky diodes, there is still low level 3rd harmonic in the circuit. The low-high impedance filter are placed within the channel waveguide between the input and output waveguides which is used to match the diodes and prevent the 2nd and 3rd harmonics (idler frequencies) from leaking into the input waveguide. 2nd and 3rd harmonics are cut off by the output waveguide and trapped in the diodes circuit. Also, the dimension of the chip channel and the suspended microstrip line are optimized to trap the idler frequencies in the circuit.

B. Design Methodology

The methodology used for the design uses a combination of

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non-linear circuit simulations (Agilent ADS) and 3D electro-magnetic simulations (Ansoft HFSS) that is based on the methodology presented in [8],[9]. To start with, a standard diode model customized with in-house parameters was implemented together with its close 3D passive environment (diode cell), plus ideal input and output matching networks. During this simulation, the anode zero junction capacitance and the diode cell geometry, including anodes positions, input channel width and input stub length, were optimized using the harmonic balance and optimization routines of ADS in order to reach optimum power efficiency. Then, each transition in the circuit including step impedances, coupling probes and waveguide transitions were simulated within the 3-D electromagnetic environment with appropriate boundaries, waveports assignment and de-embedding planes. The simulation outcomes (2-D S-parameter matrices and their attenuations, impedances and permittivity values at central uided frequencies) were used in a global non-linear optimization. During this second optimization step, ideal $\lambda/4$ initial lengths were defined in the step-impedance filter and matching network in order to converge to optimum lengths of the circuit transmission lines. Several iterations were necessary to define the appropriate dimensions of the position of the input back-short, the diodes geometry, the input probe and the output probe near the diodes in order to reach a wide impedance matching over the input frequency band. Finally, the values found during the previous steps were feed back in HFSS to build the full circuit structure as shown in Fig. 1, and the circuit was finally simulated with the harmonic balance routine to check the coupling efficiency, global efficiency and output power. The electrical parameters of the Schottky diode model considered in the simulations are a series resistance Rs =30 Ω, an intrinsic zero voltage junction capacitance of Cjo = 1.6 fF, an ideality factor =1.3 and a built-in potential Vbi = 0.8 V. This design was optimized for 5.5 mW of input power and -1 V bias included.

III. FABRICATION AND ASSEMBLING

A. *Circuit fabrication*

As described in the previous section the fabricated quadrupler circuit features two diodes integrated on a 5 um thick GaAs membrane. The membrane epitaxial layers were grown by MBE technique, fine structures, like the anodes and the air-bridges were using the electron beam lithography for its highest precision. The anodes are about 0.6 um × 0.6 um, the mesas are about 7.6 um, and the doping of the epilayer is 5×10^{17}. The gap between the edges of the anode and the ohmic contact was set to about 0.7 um. The chip is inserted between the input and the output waveguides in a channel of 93 um × 52 um cross section and approximately 232 um long.

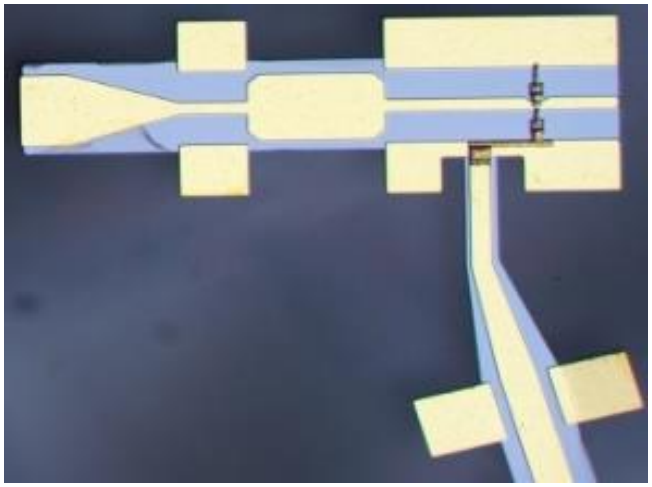

Fig.2. 750–1100 GHz circuit with beam-lead

B. *Circuit assembling*

The beam leads are thin gold layers that allow suspending the circuit in the channel without using conductive glue or golden bonding. The membrane circuit has been assembled into one of two halves and the beam leads are thermo-compressed on the block. The introduction of beam provides more precise RF and DC grounding and takes the significant improvement during the chip handling and assembling into the blocks. Protruding part of the chip is the DC line for biasing. It can also be used to grab the chip during the chip assembling into the blocks.

IV. MEASUREMENT

A. *DC characteristic*

Before electrical assembly, I-V on-wafer measurement have been performed, giving excellent diode I-V curve and ΔV, with the ΔV defined as ΔV = V (I=100 μA) - V (I=10 μA) = 72 mV. The extracted electrical parameters of the Schottky diode from the curve fitting are: series resistance R_s = 18 ohms, an ideality factor η = 1.27, and a built-in potential of V_{bi} = 0.78 V. The series resistance here is larger than the value mentioned in section II, which is partly due to the anode diameter after the fabrication is 0.8 um × 0.8 um rather than the value of 0.6 um × 0.6 um in simulation procedure.

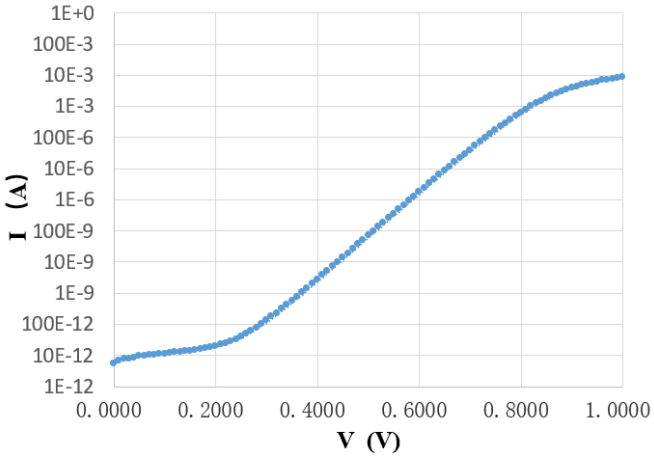

Fig.3. Diode I-V curve

B. RF characteristic

Another test measures the output power performance of the full band quadrupler. As illustrated in Fig.3, the power measurement gives -28 dBm minimum power across the 750-1100 GHz band, with -13dBm peak output power at 950 GHz. The measurement has very similar trend and a good fit to the design simulation results[11].

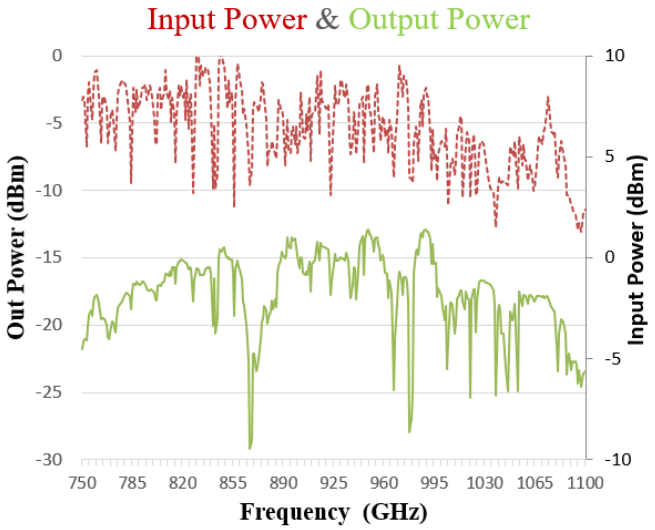

Fig.4. 750–1100 GHz circuit performance

C. Comparison to Previously Published Results

Table I provides a comparison of the current results against published quadruplers.

TABLE I
COMPARE WITH SIMILAR WORKS

Reference /Year	Technology	Bandwidth	Output Power
[12]/2014	0.13 μm SiGe HBT	50 - 75 GHz	-1 dBm
[13]/2014	0.12 μm SiGe BiCMOS	70 - 110 GHz	-1.5 to 2 dBm
[14]/2020	0.25 InP DHBT	110 - 130 GHz	5 to 7 dBm
[15]/2014	quasi-vertical diode	140 - 170 GHz	12 to 18 dBm
[16]/2013	45 nm SOI CMOS	275 - 285 GHz	-7 dBm
[17]/2015	45 nm SOI CMOS	390 - 440 GHz	-10 dBm
[18]/2012	35 nm mHEMT	435 - 480 GHz	-14.3 dBm
[19]/2017	Schottky barrier diode	322 - 345 GHz	0 dBm
[20]/1984	Schottky barrier diode	310 - 345 GHz	-3 dBm
[21]/1979	Schottky barrier diode	589 GHz	-28 dBm
This work	Schottky barrier diode	750 - 1100 GHz	-28 to -13 dBm

V. Conclusion

The Schottky diodes on GaAs membrane were fabricated with a process entirely based on electron-beam lithography. The performance shows its potential to be used as the extended parts for terahertz vector network analyzer.

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