HMMC-5040

20-40 GHz Amplifier

Reliability Application Note # 46

March 1995

This application note describes the reliability and environmental tests which have been performed to date on the HMMC-5040 amplifier. Engineering analysis and some reliability conclusions are provided to aid designers in the consideration and proper use of this amplifier in a reliable end product. The information provided is considered typical data and should be considered supplemental to the HMMC-5040 data sheet.

Topics covered:

1.0 Thermal resistance
2.0 HTOL testing
3.0 RF Stress
4.0 ESD Stress

1.0 Thermal Resistance

A thermal modeling program was used, in conjunction with liquid crystal thermography, to determine the thermal resistance and to study the thermal profile of the HMMC-5040 amplifier. The thermal modeling tools are especially useful for the short gate length PHEMT process where liquid crystal measurements are difficult and tedious to perform. The accuracy of the modeling system, on the circuit level, is a result of developing the individual device models from extensive thermal testing done on representative process monitoring devices. Each of the representative process monitor devices, both active and passive, have been thermally characterized as part of the reliability qualification phase of the PHEMT process development. The accuracy of the circuit level thermal modeling program has been verified and the results correlated to the fab process monitors.

The thermal resistance of GaAs ICs varies as a function of the circuit backside temperature. Table 1 provides the thermal resistance (θ) of the HMMC-5040 at three backside temperatures (T_{bs}). Channel temperature (T_{ch}) is calculated from the equation:

$$T_{ch} = \theta \times P_d + T_{bs}$$

Table 1. Thermal Resistance

T_{bs} (°C)	θ (°C/W)	T_{ch} (P_d = 1.35W[1])
-55	41	0
+25	53	96
+75	62	160

[1]$P_d = V_d \times I_d = 4.5\ V \times 300\ mA = 1.35\ W$

The thermal resistance at a desired backside or channel temperature can be estimated from the table values and the ratio:

$$\theta_1/\theta_2 = T_1/T_2$$

T is in Kelvin (°C + 273)

2.0 HTOL High Temperature Operating Life

HTOL testing was performed during the qualification phase of the HMMC-5040 amplifier. The HTOL tests stressed 24 devices from two different wafers. The circuits were biased at V_d = 4.5V, I_d = 300 mA, and the circuit's ambient temperature was elevated to result in a 280°C channel temperature. Periodically during the HTOL stress, the devices were removed and a variety of DC and RF data were taken. These tests concluded at 500 hours with no failures. Table 2 provides a summary of these tests.

Table 2. HTOL Test Summary

Parameter	Failure Criteria	Max. Drift @ 500 hrs.
S_{21}	±3 dB	-1.5 dB
I_{ds}	<10% Drift	~5%
P_{out}[1]		<±1 dB

[1]P_{out} measured at a variety of power levels, frequencies, and biases.

The purpose of these accelerated stress tests is to extrapolate a median life expectancy under normal stress conditions from failure data at high stress. In these tests, the acceleration factor is temperature.

During development of the PH9A process, representative process monitor FETs were HTOL tested at two channel temperatures in order to determine their activation energy. The activation energy for these representative active devices was determined to be 1.6 to 2.3 eV. Figure 1 is a graphical representation of the Arrhenius method which is used to project the life line for the HMMC-5040. The life line uses the 1.6 eV activation energy to determine its slope. There were no failures of the 24 circuits tested at the end of 500 hours. Using 500 hours as a worse case MTTF (MTFF is the time required for 50% of the devices to fail) at T_{ch} = 280°C, the lifeline extrapolates to 10^6 hours at T_{ch} = 160°C.

3.0 RF Stress

The HMMC-5040 data sheet specifies that the circuit will withstand 21 dBm continuous maximum input power. This is stated as the Absolute Maximum Rating and this power level should not be exceeded at the rated channel temperature of 160°C. Circuit degradation may occur above this level, resulting in reduced performance.

Circuits were tested to determine the RF input power level to induce catastrophic failure; the catastrophic level was 27 dBm. In all cases, the failure mechanism was burnout of the 50 ohm input matching resistor.

4.0 ESD Testing

It is well known that GaAs ICs are sensitive to ESD. Proper precautions and ESD protection techniques should be used when handling these circuits. The HMMC-5040 was tested for ESD sensitivity. These tests were performed on four circuits mounted and bonded in a single 24 pin package. The circuits were unbiased. The backside was grounded and ESD voltage was applied to each open pad in 50 volt increments. After each 50 volt increment, the device was biased and the input leakage current was measured. The failure criteria was >5% change in leakage current. The worse case (i.e., lowest voltage) failure from these tests was +600 volts applied to the RF output port.

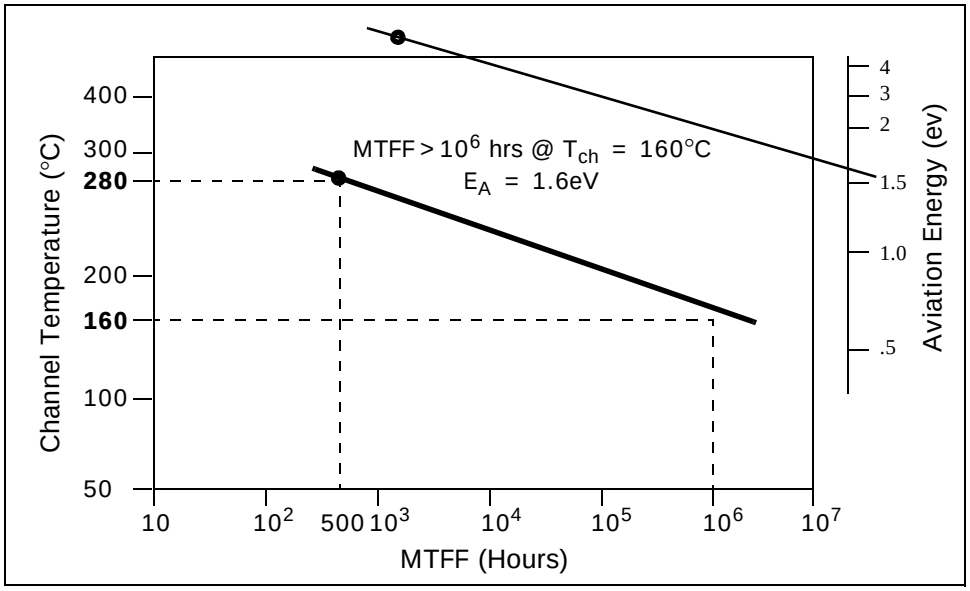

Figure 1.
HMMC-5040 Arrhenius Plot