# SPECTRAL PROCESSOR FOR THE 300 FOOT TELESCOPE

## OVERVIEW AND PROGRESS REPORT

Richard J. Lacasse

March 10, 1987

### Introduction:

For some time now a new spectrometer for the 300-foot telescope has been in the design and construction phase. Dubbed the Spectral Processor, it is intended to satisfy many of the needs of both the spectral line and pulsar communities. This report provides a reasonably detailed overview of the Spectral Processor as well as a progress report.

### Overview:

The Spectral Processor is intended to serve both the spectroscopist and pulsar observer. Hence, the major design goals of this project are the following:

1 - Adequate frequency resolution and bandwidth for spectroscopy (<=1024 points, <=40 MHz);
2 - Adequate time and frequency resolution for pulsar observations (>=12.8 usec, 4 IF channels at 256 frequency points each);
3 - Real-time dedispersion, stokes parameter calculation, and faraday rotation correction capabilities.
4 - RFI rejection and tolerance;
5 - Two effectively independent spectrometers with multiple inputs;
6 - Flexibility in many respects.

The implementation that has been conceived to satisfy these goals consists of two, effectively independent, high time resolution FFT spectrometers. Several modules, arranged in a pipelined architecture, are required to satisfy all the goals stated above. These are shown in the attached block diagram. In studying the block diagram, several points are worth keeping in mind. Firstly, the diagram shows all the control electronics, but only one of the spectrometers. Secondly, most of the specified modules can be bypassed, although this is not shown to avoid cluttering the diagram any more than it already is. Thirdly, each of the two spectrometers is designed for up to eight IF inputs. Finally, the Biplex FFT module can implement various length transforms, from 128 to 1024 points. Each module is described below (for aficionados only!):

IF to Video Converters: These modules provide a variety of analysis bandwidths from 40 MHz to 78 kHz, and an RFI detector. In order to achieve high RFI immunity, the design goal for rejection of the unwanted sideband is 40 dB. The full-blown design calls for 16 converters although only 8 (4 for each pipeline) will be built due to budgetary constraints.

Six Bit ADC: A full complement of 16 high speed ADC's is in hand. These use a commercial board with some minor modifications.

ADC Interface: This module accepts inputs from up to 8 ADC's at up to 80 Ms/s and reformats the data into four streams at up to 20 Ms/s. Obviously not all the samples from all the converters are passed through to the Buffer Memory; only combinations that do not exceed the maximum data rate of the Buffer Memory are allowed.

Buffer Memory: The Buffer Memory accepts sampled data from the ADC Interface, double buffers it, and reads it out in bit-reversed order to satisfy the input requirements of the FFT modules. Although all IF channels are sampled simultaneously, they are read out of the Buffer Memory in channel sequence, effectively time multiplexing the FFT.

Window Multiplier: This module multiplies the data by a user selectable window that allows the user to trade resolution-bandwidth for RFI immunity and dynamic range.

Biplex FFT: This block consists of 10 radix two "butterfly" modules (plus one hot spare) which implement a standard FFT architecture. Resolution of data and trigonometric coefficients is 16 bits. Transforms of less than 1024 points are accommodated by switching out modules. A 1024 point complex spectrum can be produced each 25.6 usec.

Real Correction: This module implements a standard correction required when feeding a complex FFT real data points masquerading as complex data.

Square or Cross Multiply: This module produces power spectra from the voltage spectra. When data rates permit, both self and cross power products can be computed.

Stokes Multiplier: This module computes stokes parameters in real time from the square and cross products.

Faraday Correction: This module is used to correct for faraday rotation across the spectrum. Coefficients are down-loaded from the control computer.

Accumulator and Dedisperser: This module's flexible design makes possible a variety of accumulation modes. Some of the possible modes include standard signal/reference averaging, dedispersed averaging, and averaging in many time and frequency bins synchronous with a pulsar. In addition, RFI contaminated data can be rejected on a per transform basis, and counts of rejected data are kept for later normalization.

Synthesizer: This is a commercial unit whose purpose is to allow the calculation of an integral number of transforms within a pulsar period.

Timing Generator: The timing generator produces clocks and timing reference signals required by various modules.

Controller: This module acts as an intelligent interface between the MASSCOMP and the rest of the Spectral Processor. It must down-load control information to the Spectral Processor modules, monitor the status of the various modules and subsystems, and report back to the MASSCOMP.

## Progress Report

The primary goal of this project is to have a usable instrument turned over to the users in a timely fashion. It is expected that this goal will be met late in 1988. The immediate goal, however, is to design and build half the system, i.e., one spectrometer plus control, in order to run system tests. This tactic should lead to a more efficient realization of the primary goal. A short summary of our progress towards achieving the immediate goal follows:

Complete: ADC's, Buffer Memory, Window Multiplier, initial FFT module, Timing Generator.

In progress: ADC Interface, making 11 copies of the FFT module, Controller, Accumulator, and IF to Video converters.

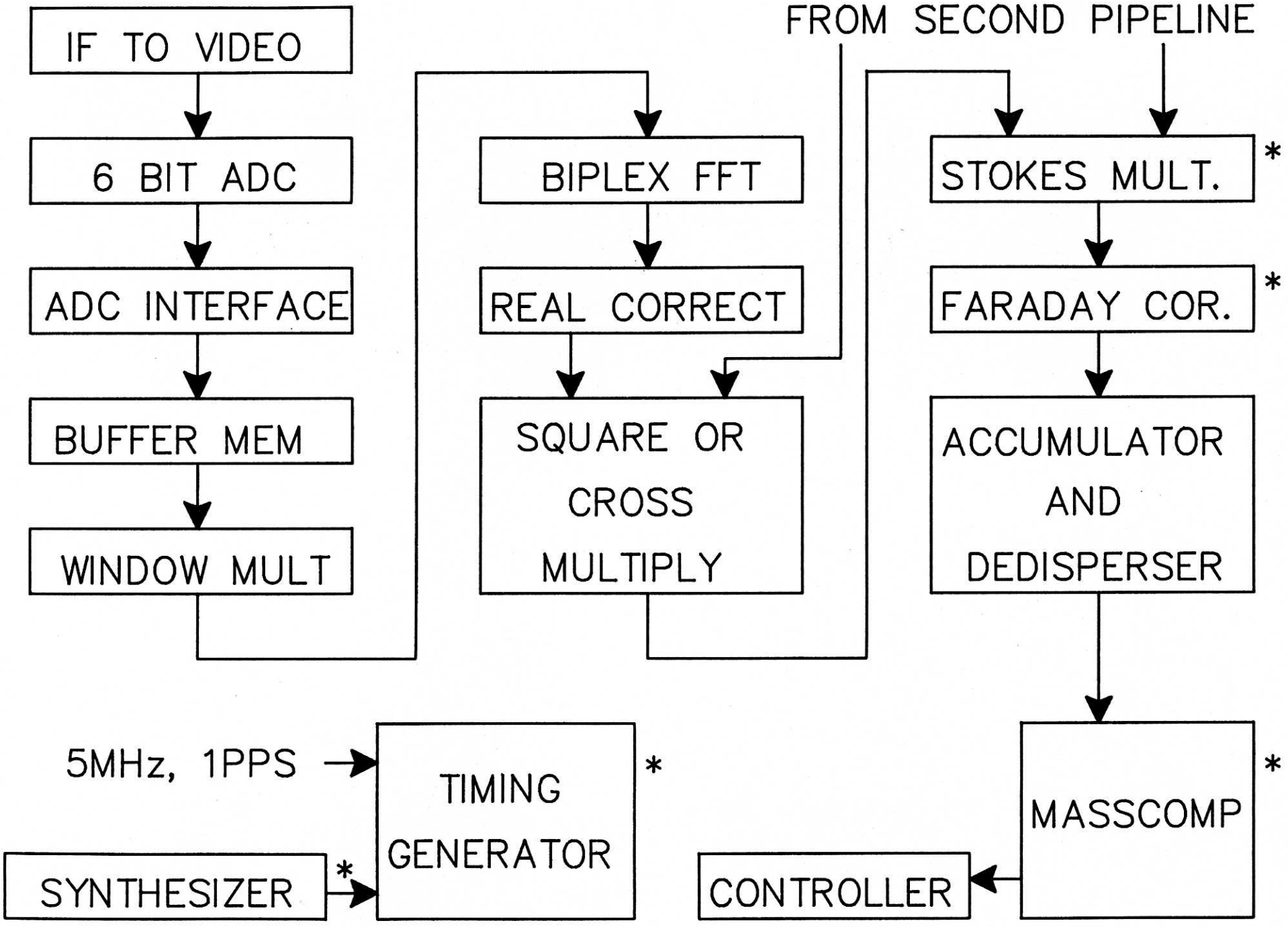
To be done: Real Correction, Square or Cross Multiply, rack design, and control and analysis software.

Deferred: Stokes Multiplier, and Faraday Correction. (To be designed and built after initial system is turned over to the users.)

Completing the second half of the system once the first half has been built and debugged is straightforward and should not take very long.

Attachment

# SPECTRAL PROCESSOR BLOCK DIAGRAM




* COMMON TO BOTH PIPELINES

NOTE : ONLY ONE DATA PIPELINE SHOWN