Subject: RE: WBS for Joint Phase 1 Date: Mon, 4 Oct 1999 16:45:10 +0100 From: R.Wade@rl.ac.uk To: baudry@observ.u-bordeaux.fr CC: rkurz@eso.org, guillote@iram.fr, rbrown@NRAO.EDU, pnapier@NRAO.EDU

Alain

This just to confirm that I have set funds aside to cover the Jodrell work on both the IF transmission and the advanced correlator study.

Final allocation is clearly subject to the exact level of their request, particularly for the equipment needed for the fibre study, but from our preliminary discussions I don't foresee any big problems. The main requirement now is for Jodrell to reach agreement with yourself and Dick Sramek. Once this is concluded I should be able to arrange funding very rapidly.

Regards Richard

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-----Original Message-----From: Baudry Alain [mailto:baudry@observ.u-bordeaux.fr] Sent: 04 October 1999 11:27 To: rkurz@eso.org; Stephane Guilloteau; Richard Wade; Robert Brown; Peter Napier Subject: WBS for Joint Phase 1

Dear Dick,

I must say I have not received so far all the answers I had hoped, including answers I desperately need from John Webber; but I see him in soon.

Nevertheless and because you leave on the 4th I pass you some comments to help.

** First I'd like to add to the general WBS

7,4 Preliminary Design of Future Correlator

I suggest the following sub-elements

741 High Speed Sampler Prototype742 High Speed FIR Filter Prototype743 Phase 1 Feasibility Study of Future Correlator744 Phase 1 Preliminary Design of Future Correlator

I know that 741 and 742 could be seen as redundant with 731 and 732 in 7,3 Baseline Correlator Development, but I have not been able to exchange in depth with John W. on this question.

** Our activities in Europe cover part of Task 6 'IF/Transmission Subsystem'. In task 6 the UK group at Jodrell, D. Sramek and I have well interacted ...but not been able to conclude yet. Detailed work packages on FO links still require iterative discussions and final agreement of R. Wade, D. Sramek and me.

Still subject to negociations: the level of funding at Jodrell with funds administrated by R. Wade.

The work headed by B. Anderson and R. Spencer at Jodrell will fall inside Task 6,3 FO Design and Development and more specifically in 631 and 632; but this depends on your AEC decisions.

See you soon in Washington, Alain

* 6 IF/Transmission Subsystem

* Task 6,3 FO Design and Development Responsible
* 631 FO Design & Specification
Analog & digital link designs & budgets Anderson
Separate fibres versus wave miwing schemes Spencer
Laboratory measurements: high speed digital links, (sync., RFI); amplitude and phase stability of analog systems Spencer
* 632 IF Transmission

Sampling schemes for digital links:4-bit/2-bit samples; data framing/reframing; system synchronisation Anderson

I am afraid I can't give now a time sacle for the above work which can start this fall.

* 7 Correlator

* Task 7,4 Preliminary Design of Future Correlator

* 741 High Speed Sampler Prototypes Date, Responsible Technical Specifications, Tasks in Other Institutions 0ct - Nov 99 Baudry **Review of Commercial Devices** Oct - Nov 99 Deschans Feasibility Study (2-bits, 4-levels) Oct 99 - March 00 Deschans Parallel Feasibility Study (3-bits) Feb 00 - June 00 Begueret Preliminary Design Phase > March 00 Deschans Final Design Review Jan 01 Baudry et al. **ASIC** Prototype Production & Tests (BiCMOS SiGe technology, O.25 um) - first run and tests < April 01 Begueret - other runs and tests <Oct 01 Begueret Final Report Oct 01 Key milestones: Final Design Review in Jan 2001 First run for ASIC production & tests _____ * 742 High Speed FIR Filter Prototype Date, Responsible Simulations: number of sections, low-pass and band-pass FIRs, 2-bit resampling etc. Oct 00 - Jan 00 Anderson Report on Digital LO Configuration Jan 00 Comoretto FIR Filter with FPGA Chips Oct 99 - Jan 00 Cais FPGA Selection, High Speed FIR filter Dec 99 - May 00 Picard

(remember I don't want to give too many details as I consider the real start of investigations is our first meeting of 19, 20 and 21 October)

Responsible

Top Level Specs. versus Requirements Baudry

Global Architecture: system design options; modularity; identification of critical areas and technologies Bos/Torres

Correlator Model: interface to IF, station and baseline electronics Bos/Torres

Delay Tracking and FIRs

Fringe Stopping

Fast Interconnection Schemes: envisioned technologies,documentation, designs versus cost Torres

Correlator Chip: investigations relevant to design & technologies Anderson

Correlator Boards: investigations relevant to design & technologies Comoretto

Signal Distribution: frequency and clock

Design Tools, IC Technologies & Implementation Bos/Whitney

System Verification & Tests: softaware, requirements on architecture

Feasibility Review and Report: proposed architecture & design, first cost & manpower estimates, planning Baudry et al.

Key milestone: Feasibility Review around December 2000

* 744 Phase 1 Preliminary Design of Future Correlator Approximate Duration: December 2000 - November 2001 Solidification of Architectural Concept Bos/Torres Proposed Design & Documentation **Bos/Torres** Fast Interconnection Schemes: selection of technologies Torres Alternative Technical Solutions **Correlator Chip Specifications** Anderson IC Development & Design Tools Bos/Whitney Outline of Custom Board Design Comoretto Control & Test Software Solidification of Cost & Staff Estimates Preliminary Design Review & Report _____

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