

Subject: RE: WBS for Joint Phase 1
Date: Mon, 4 Oct 1999 16:45:10 +0100
From: R.Wade@rl.ac.uk
To: baudry@observ.u-bordeaux.fr
CC: rkurz@eso.org, guillote@iram.fr, rbrown@NRAO.EDU, pnapier@NRAO.EDU

Alain

This just to confirm that I have set funds aside to cover the Jodrell work on both the IF transmission and the advanced correlator study.

Final allocation is clearly subject to the exact level of their request, particularly for the equipment needed for the fibre study, but from our preliminary discussions I don't foresee any big problems. The main requirement now is for Jodrell to reach agreement with yourself and Dick Sramek. Once this is concluded I should be able to arrange funding very rapidly.

Regards
Richard

Richard Wade
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-----Original Message-----

From: Baudry Alain [mailto:baudry@observ.u-bordeaux.fr]
Sent: 04 October 1999 11:27
To: rkurz@eso.org; Stephane Guilloteau; Richard Wade; Robert Brown; Peter Napier
Subject: WBS for Joint Phase 1

Dear Dick,

I must say I have not received so far all the answers I had hoped, including answers I desperately need from John Webber; but I see him in soon.

Nevertheless and because you leave on the 4th I pass you some comments to help.

** First I'd like to add to the general WBS

7,4 Preliminary Design of Future Correlator

I suggest the following sub-elements

Design of FIR/LO Board < June 00
Comoretto

Test Board for Evolved Digital FIRs < Sept. 00
Picard

Design Review Oct. 00

ASIC Design, Fabrication & Tests (with
dedicated demonstrator) Oct. 00 - June 01

Ket milestones: Design review
First ASIC production & tests around March 01

* 743 Phase 1 Feasibility Study of Future Correlator

Duration Oct. 99 - end 00

(remember I don't want to give too many details as I consider the real
start of investigations is our first meeting of 19, 20 and 21 October)

Responsible

Top Level Specs. versus Requirements Baudry

Global Architecture: system design
options; modularity; identification
of critical areas and technologies Bos/Torres

Correlator Model: interface to IF,
station and baseline electronics Bos/Torres

Delay Tracking and FIRs

Fringe Stopping

Fast Interconnection Schemes:
envisioned technologies,documentation,
designs versus cost Torres

Correlator Chip: investigations
relevant to design & technologies Anderson

Correlator Boards: investigations
relevant to design & technologies Comoretto

Signal Distribution:frequency and clock

Design Tools, IC Technologies
& Implementation Bos/Whitney

System Verification & Tests: software,
requirements on architecture

Feasibility Review and Report: proposed architecture & design,
first cost & manpower estimates, planning Baudry et al.

Key milestone: Feasibility Review around December 2000

* 744 Phase 1 Preliminary Design of Future Correlator

Approximate Duration: December 2000 - November 2001

Solidification of Architectural Concept Bos/Torres

Proposed Design & Documentation Bos/Torres

Fast Interconnection Schemes:
selection of technologies Torres

Alternative Technical Solutions

Correlator Chip Specifications Anderson

IC Development & Design Tools Bos/Whitney

Outline of Custom Board Design Comoretto

Control & Test Software

Solidification of Cost & Staff Estimates

Preliminary Design Review & Report

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