A New Pillar Geometry for Heterostructure Barrier Varactor Diodes

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Abstract

We report on a novel diode geometry, with reduced thermal resistance, for Heterostructure Barrier Varactor, HBV, diodes. The pillar geometry presented here involves the complete removal of the substrate, electrical contact is made by the forward and reverse side processing of metallic pillars.
We propose that there is a limit to the maximum number of barriers that can be used to increase the power capability of a HBV. An analytical model has been developed to study these effects. In considering the case of a perfect thermal heat sink the limit is found to be fourteen, in applying this model to the new pillar structure this is reduced to six.

1) Introduction

The Heterostructure Barrier Varactor, HBV, has received considerable attention since its proposal in 1989 by Kollberg and Rydberg [1]. The HBV is a symmetric varactor which gives rise only to odd harmonic generation, simplifying the circuit geometry for higher harmonic multiplication, due to the absence of idler circuits. For this reason, together with the ability to epitaxially stack any number of these devices and increasing the power handling capacity, recent results are comparable with the best reported Schottky based multipliers [2-5].

Present interest in HBV frequency multipliers is focused towards changes in the device geometry and increased integration. A variety of material systems are used, and theoretical work continues with the goal of increasing the capacitance modulation whilst reducing the conduction current. However, theoretical and experimental results continue to show the domination of thermal effects.

As the intrinsic HBV temperature is raised, the conduction current, which results primarily from thermionic emission over the barriers, increases. This increase in conduction current reduces the capacitance modulation. Hence, together with the increase in series resistance, the overall device efficiency is reduced. Moreover, the breakdown voltage decreases with temperature, reducing the power handling capacity [6]. These effects are well known and reflected by the many device designs in which the thermal impedance is of considerable importance.

In this paper we demonstrate a new pillar diode geometry which is optimised for a reduction in the thermal resistance. Our results suggest a limit to the number of barriers; this limit is based on the dominance of thermal effects.

2) Pillar Geometry

2.1) Device Concept

With the move from whisker to planar devices, the twin air-bridge structure has become a popular fabrication process for HBV diodes. Typically, the thermal impedance from the edge of the mesas, contacted via air-bridge technology on a flip-chip, to the multiplier block is estimated to be of the order 0.7 K/mW [7]. The thermal conductivity of the substrate and the length of the bond fingers give the main limitations to the thermal resistance. The latter of these must also be optimised with respect to the parasitic capacitance, such that a decrease in their length reduces the thermal resistance at the cost of increased parasitic capacitance.

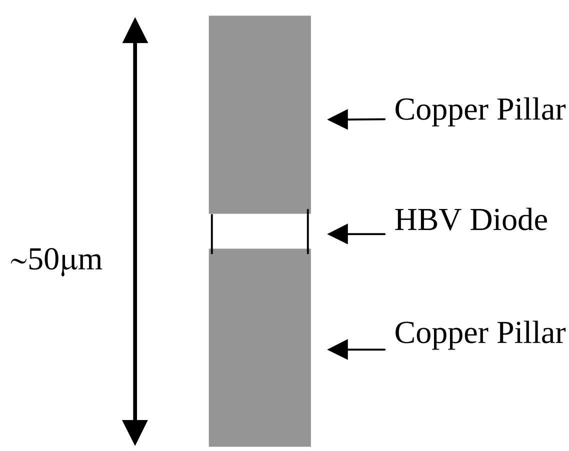

Figure 1) Schematic diagram of pillar HBV structure.

The new pillar geometry presented here is conceptually very simple. The semiconductor mesa is contacted symmetrically by two metallic pillars, and all other substrate material is removed. Figure 1 shows a schematic of the pillar structure.

This structure can be soldered directly into a circuit or, as is planned, soldered into a flip-chip and mounted in the traditional planar manner. A schematic of this structure is shown in figure 2. The estimated thermal contact resistance of the pillar structure, when soldered into an adjoining flip-chip, is 0.2 K/mW.

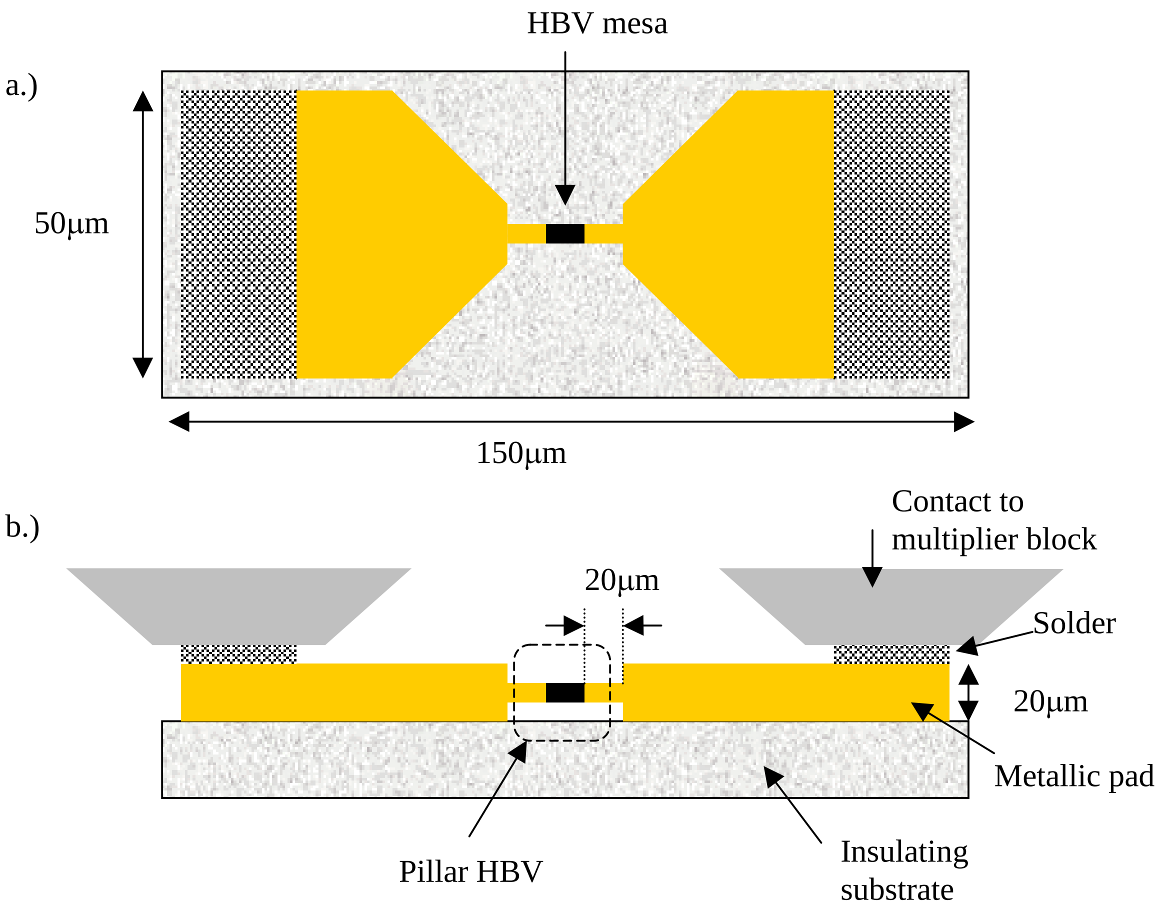

Figure 2) Top (a.) and cross-sectional (b.) representation of flip-chip mount for pillar HBV.

One of the significant advantages the twin air-bridge structure has over alternative approaches is the fact that two mesas are electrically contacted back-to-back. Asymmetries within the epi-layers are effectively cancelled; however, this is at the cost of increased series and spreading resistance formed in the connecting n^+ region. These terms together represent a significant fraction of the total electrical resistance. This new geometry is, therefore, reliant on good quality material with symmetrical material characteristics. However, the resulting electrical and thermal resistances are significantly reduced, together with the parasitic capacitance. The on-wafer device density also approaches the maximum possible value; the most significant wastage derives from edge-bead effects during fabrication.

2.2) Device Fabrication

The HBV material structure, ITME 1817, shown in Table 1,was grown by MOVPE. The device fabrication was performed using standard photolithography techniques and alloyed ohmic contacts. The mesa was initially etched by chlorine based Reactive Ion Beam Etching, RIBE, followed by a short wet etch. Thick film resist was used to define the top side pillar structure which was copper electroplated to the top level of the resist. An additional sputtering process was employed before electroplating a sacrificial copper substrate to ~50µm. The InP wafer substrate was subsequently removed by wet chemical etching. Evaporating the contact metalisation and repeating the pillar electroplating process was the final stage of the device fabrication. The devices were separated by carefully etching the sacrificial substrate. A single device soldered on a gold-on-quartz filter can be seen in figure 3.

Table 1
The HBV Material Structure (ITME 1817)

Layer	Material	Doping [cm^{-3}]	Thickness [Å]
Contact	InAs	$>5x10^{18}$	100
Contact	$In_{.53\rightarrow1}Ga_{.43\rightarrow0}As$	$>5x10^{18}$	6000
Modulation x 6	$In_{.53}Ga_{.47}As$	$3x10^{16}$	4000
Spacer x 6	$In_{.53}Ga_{.47}As$	undoped	200
Barrier x 6	$Al_{.48}In_{.52}As$	undoped	50
Barrier x 6	AlAs	undoped	30
Barrier x 6	$Al_{.48}In_{.52}As$	undoped	50
Spacer x 6	$In_{.53}Ga_{.47}As$	undoped	200
Modulation	$In_{.53}Ga_{.47}As$	$3x10^{16}$	4000
Contact	$In_{.53}Ga_{.47}As$	$>5x10^{18}$	3000
Substrate	InP	N^{++}	

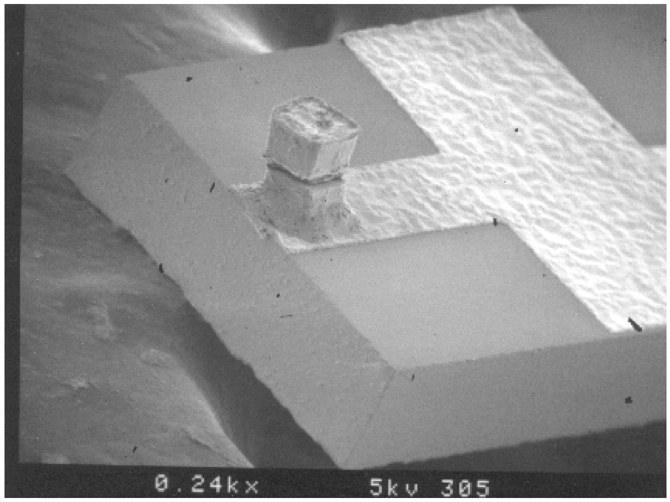

Figure 3) Pillar HBV structure soldered on a gold-on-quartz filter.

3) Thermal Estimations

3.1) Thermal Models

In this section, we propose that a limit exists for the maximum number of effective barriers for the HBV. Based on first order approximations and steady-state thermal analysis, it is argued that additional barriers beyond this limit act predominately as electrical series losses. The value of this limit is also shown to be dependent on the external thermal contact resistance.

We have solved the one-dimensional temperature profile analytically in a section of GaAs given a point source and a distributed source of power dissipation, this has been combined with linear and nonlinear models for the thermal conductivity of GaAs. The nonlinear thermal conductivity is as follows;

$$K_{GaAs} = \frac{A}{T^{1.2}} \quad (1)$$

where the constant, A, varies with doping. For GaAs doped at N_D=1x10^{17}cm^{-3}, A=48800 [8], which we have used here. In the linear model we assume a fixed temperature of 300K.

The temperature differential developed over a section of material is calculated as the product of the thermal power flow through and the thermal resistance of the element. The

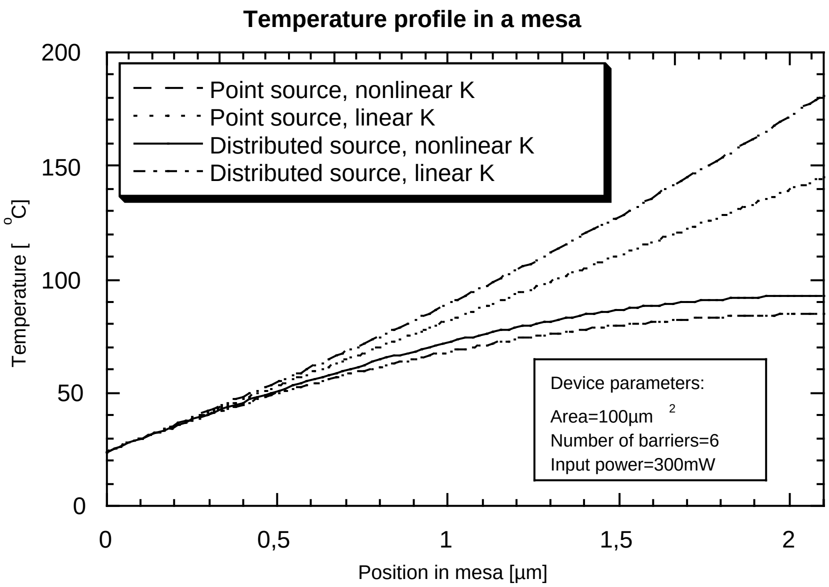

Figure 4) Comparison of thermal models.

thermal resistance of a bulk section of material surrounded by air can be solved directly as

$$R_{Thermal} = \frac{t}{K\pi r^2} \tag{2}$$

where t is the thickness of the section, K is the material's thermal conductivity and r is the equivalent radius based on the cross-sectional area of the section.

Evaluation of the above formulae reveal four distinct trends, which are plotted in figure 4 for typical values of area, number of barriers and input power for a moderately high powered HBV. It is also assumed that one edge of the mesa is at room temperature and that the total heat flow, resulting from the power dissipation in the active region, is in one direction only, towards the heat sink. Although the values taken are appropriate from an electrical prospective, by ignoring the contacting geometry, the temperature scale is in effect arbitrary. In estimating the mesa thickness, L, we have assumed a typical modulation layer thickness, l, of 300nm together with the relationship

$$L \approx l(N+1) \tag{3}$$

where N is the number of barriers. Hence, assuming the contact and barrier layers to be of negligible thickness. The power dissipated thermally in the device is approximated to the input power.

The model involving a distributed power source with nonlinear thermal conductivity was considered as the most appropriate for the analysis which follows. Under these assumptions, the temperature, $T(x)$, at point x, for a mesa of length, L, and equivalent cross-sectional radius, r, is given by

$$T(x) = \left(\frac{1}{T_0^{0.2}} - \frac{0.1\left(2Lx - x^2\right)P_{Total}}{LA\pi r^2} \right)^{-5} \quad \text{for} \quad 0 \le x \le L \qquad (4)$$

where T_0 is the temperature of the mesa at the heat sink. P_{Total} is the total power dissipated in the active region.

3.2) Operating temperature of Pillar HBV diode

Thermal analysis of the pillar HBV structure is simplified by the symmetry of the device. For a given dissipated power and mesa length we are able to solve for half the power dissipated by half the length of the mesa. The asymmetry of the air-bridge structure and the essentially one directional heat flow of the whisker structure, do not allow this simplification.

The temperature in centigrade at the centre of an N barrier HBV mesa is shown in figure 5; this follows from the solution of equation 4 for a symmetrically contacted device. In this figure the contact is assumed to be a perfect heat sink, such that the edges of the mesa are kept at 300K. Lines of constant peak temperature are given as a function of power density per barrier and the number of barriers. The contour lines are only shown within the approximate validity of the nonlinear model. Taking 100^0C as a reasonable maximum acceptable temperature rise in a mesa and a power density per barrier of $0.5\text{mW}/\mu\text{m}^2$, the limiting number of barriers can be estimated at fourteen. In assuming a perfect thermal contact, this analysis implies an effective maximum in the number of barriers. Incorporating the additional effect (thermal resistance) of a 20μm copper pillar, of the same equivalent radius as the mesa, reduces the maximum number of barriers to approximately six. This is shown in figure 6.

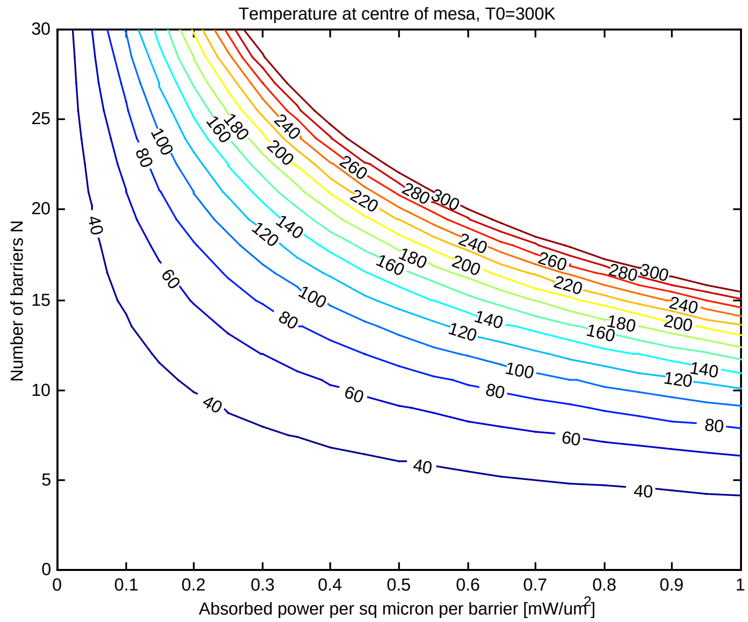

Figure 5) Temperature at the centre of a symmetrically contacted HBV mesa. The contacts are assumed to be perfectly conducting and at 300K.

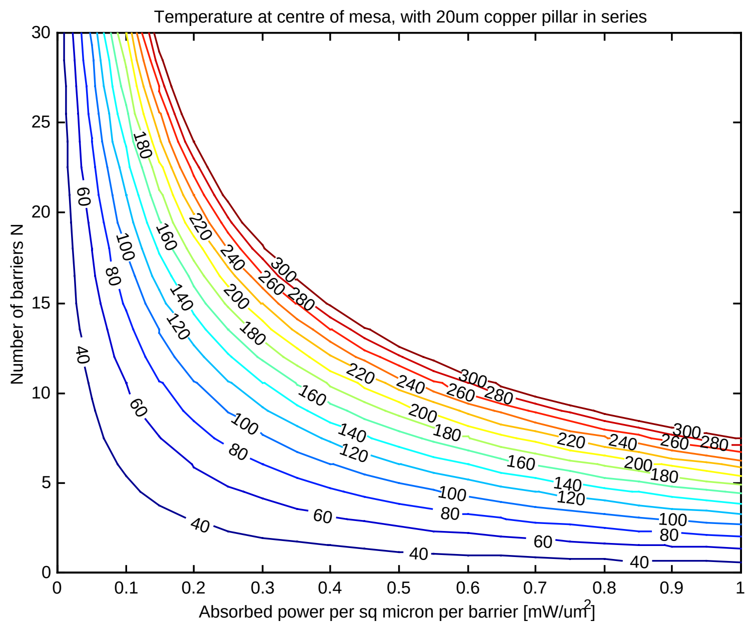

Figure 6) Temperature at the centre of a HBV mesa. The mesa is assumed to be contacted symmetrically by 20µm copper pillars to a perfect thermal conductor at 300K.

3.3) Power Handling

The analysis above is generalised in the form of power density, such that the maximum power dissipated by a symmetrically contacted HBV is linked to the area. For high powered applications, increasing the device area, for a given number of barriers, would allow higher dissipated power. However, this results in a decreased operating impedance which can present matching difficulties. The total ohmic contact resistance is also reduced with larger area such that increasing the number of barriers is usually preferable but is a trade-off with the power density per barrier.

4) Conclusions

We have demonstrated a novel device geometry for the HBV diode. These diodes have been fabricated using standard fabrication techniques, they are also robust and easy to integrate into existing circuits.

A steady-state thermal model of the HBV has demonstrated that a maximum number of barriers exists for a HBV. This is shown to be fourteen for a device contacted symmetrically by two perfect thermal heat sinks, however, this reduces to six for the new pillar structure.

The thermal approach we have taken here is by no means conclusive. No account has been taken for the output circuit delivering power at the various harmonics, nor the thermal generation in the ohmic contacts. Together, these effects represent a significant fraction of the input power. The heat generation within the diode is also a nonlinear effect where the electrical losses are strongly dependent upon temperature. A self-consistent approach involving thermal conductivity with harmonic balance estimates of individual barrier performance is required to investigate these effects further. However, we present here clear evidence, based upon thermal considerations, which indicates a limit to the maximum number of barriers for a HBV diode. Moreover, this limit is within the range typically considered for device fabrication, and therefore is an important aspect in overall device optimisation.

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