Design and Optimization of Micro-patterned Quasi-optical Impedance Transformers

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Abstract— Presented is method to model and optimize multi-layer micro-patterned impedance matching structures. For a number of geometric patterns in silicon, effective dielectric constants are calculated in the long wavelength limit using an effective capacitance method. The S-parameters of multi-layer impedance transformers are then computed using the transfer matrix method. A stochastic method known as simulated annealing is used to optimize impedance transformers and incorporate fabrication constraints. Lastly, the effective capacitance method is used to model a square pyramidal impedance taper.

INTRODUCTION

Artificial dielectric materials, such as expanded Teflon sheets, have long been used as impedance matching layers for millimeter and sub-millimeter vacuum windows, filters and lenses[1]. More recently, there has been concentrated effort to design and produce micro-patterned anti-reflection layers in silicon through deep-reactive ion etching[2]. Micro-patterned layers, also known as metamaterials, are composed of a repeated structure on sub-wavelength scales and can be characterized by an effective dielectric constant. The effective dielectric constants for grooves[3], both parallel and perpendicular to the electric field, and square posts/holes[4] have been analytically studied. We expand upon the effective capacitance method of Biber[4] to study several simple patterns in silicon. Using a stochastic optimization routine, we design a simple micro-patterned impedance transformer. Lastly, we use our method of calculating effective dielectric constants to study a square pyramidal impedance taper.

EFFECTIVE DIELECTRIC CONSTANTS

Micro-patterned materials, consisting of a repetitive pattern on scales much smaller than the wavelength of interest, can be characterized by an effective dielectric constant. This dielectric constant determines both the propagation constant of an EM wave in a layer of the material as well as the reflection and transmission at an interface between two layers of differing pattern. The effective dielectric constant of a pattern is in general polarization and frequency dependent. In the long-wavelength limit, the effective dielectric constant can be calculated using the capacitance of a single unit cell of the pattern. Fig. 1 plots the results of calculations of the effective dielectric constant

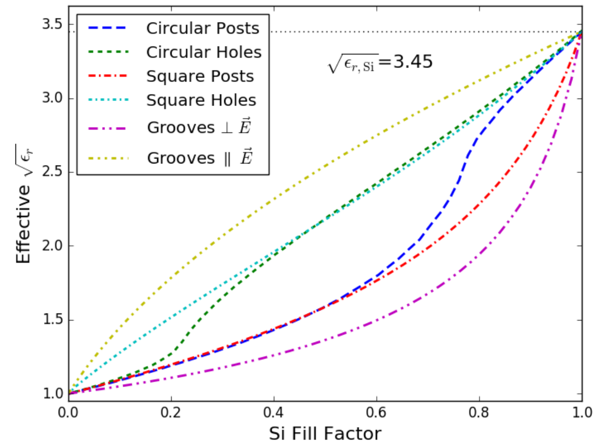

Fig. 1 Effective refractive index versus fill factor for several different patterns in silicon as calculated in the long-wavelength limit. Circular patterns experience a transition around the fill factor at which they begin to overlap with nearby holes/posts.

(plotted as the effective refractive index) for several different patterns in silicon and air as a function of silicon fill factor. As can be seen in the plot, patterns which have a continuous path of silicon along the polarization direction, such as grooves parallel to $\vec{E}$ or any variety of hole pattern, have a distinctly larger effective dielectric constant than patterns which do not have continuous silicon paths at the same fill factor.

OPTIMIZATION OF IMPEDANCE TRANSFORMERS

The S-parameters of a multi-layer micro-patterned impedance transformer can be calculated as a function of each layer's pattern geometric parameters and thickness. From the pattern parameters, polarization-dependent effective dielectric constants for each layer are calculated as described previously. Assuming a normal incidence plane wave as the impinging EM mode, we calculate the S-matrix of the multi-layer structure using the transfer matrix method[5] over the polarizations and frequency band of interest. Using the calculated S-parameters, a cost function can defined for the transformer optimization, such as a band-averaged return loss or band-worst transmission. This cost function is then minimized using a stochastic algorithm known as simulated annealing where a Metropolis-Hastings

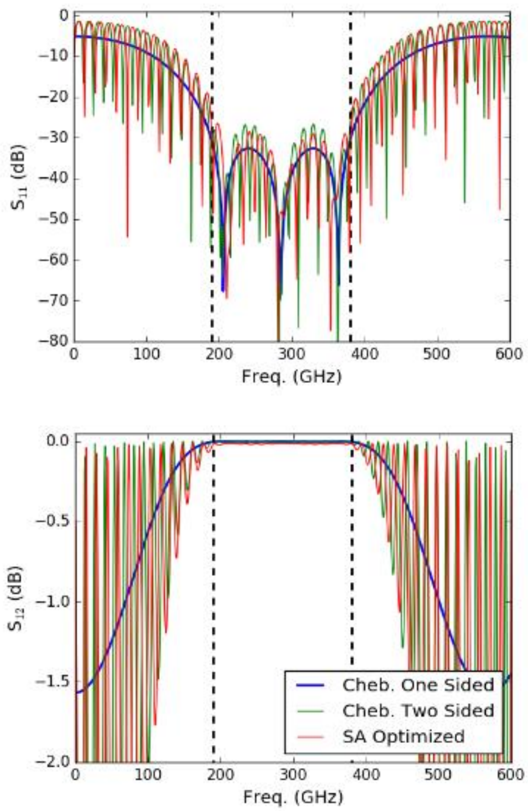

Fig. 2 Example of the results of a simulated annealing optimization of a 3-layer impedance transformer designed on a 3mm thick silicon wafer for 190-380GHz. The return loss (top) and insertion loss (bottom) are very similar to a Chebyshev transformer in this simple case, with minor improvement coming from tuning the thickness of the wafer.

algorithm is used to update layer parameters and thicknesses while the effective system temperature is slowly decreased. In this way, the layer parameters and thickness which minimize the cost and produce an ‘optimal’ transformer can be found.

Results of such an optimization are shown in Fig. 2 for a 3-layer two sided anti-reflection coating covering the 190-380GHz band on a ~3mm thick silicon wafer intended as a vacuum window. As can be seen, the result is very similar to a Chebyshev transformer in this simple case. In more complicated scenarios where the fabrication of a Chebyshev transformer is not feasible, the stochastic approach still allows for the design of an ‘optimum’ impedance transformer. Such a situation can simple arise from fabrication constraints, such as a maximum achievable aspect ratio during pattern etching.

Modeling Impedance Tapers using the Effective Capacitance Method

Tapered impedance transformers provide the ultimate in wideband performance at the cost of increased transformer length and manufacturing difficulty. Tapered square pyramidal patterns, studied in [6], can be machined in

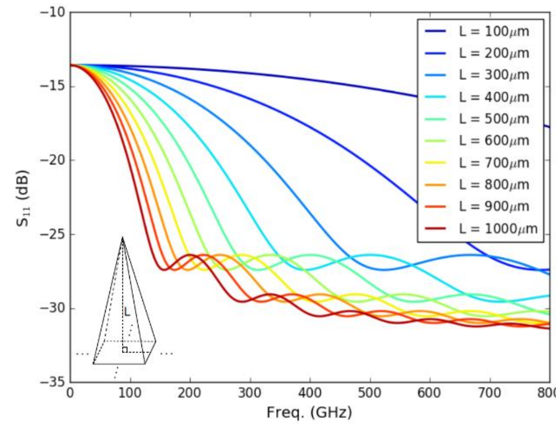

Fig 3. Simulated return loss of a 100μm pitch square pyramidal taper in HDPE as cut by a custom slitting saw. As the length of the taper increases, the cut-off frequency systematically decreases. The in-band return loss of the taper is limited by the size of the saw tip, in this simulation set to 6μm.

plastics using a custom-ground slitting saw. In order to model such a taper, the effective dielectric constants for an array of sizes of square posts was first calculated. The S-matrix of the taper was then calculated using the transfer matrix method, treating the taper as a large number of infinitesimally thin steps of square posts. In Fig. 3, we plot the simulated return loss for a square pyramidal taper of varying length. The cut-off frequency is controlled by the length of the taper, while the in-band return loss is controlled by the size of the tip of the slitting saw.

Conclusions

We have presented a simple method for the modelling and design of micro-patterned impedance transformers. In layered transformers, an effective dielectric constant is calculated for each layer. Using a stochastic approach known as simulated annealing, multi-layer transformers can be optimized over the space of layer geometric properties and thicknesses. Lastly, this method was used to study square pyramidal impedance tapers.

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