

Design and Fabrication of a Dual-Polarization, Balanced SIS Mixer Integrated Circuit

Wenlei Shan^{1*,2}, Shohei Ezaki¹, Keiko Kaneko¹, Matthias Kroug¹, Alvaro Gonzalez¹, Takafumi Kojima¹, Yasunori Fujii¹, Shinichiro Asayama¹, Takashi Noguchi¹

¹ *National Astronomical Observatory of Japan**, 181-8588, Mitaka, Tokyo, Japan,

² *Purple Mountain Observatory, 210008, Nanjing, JiangSu, China*

*Contact: wenlei.shan@nao.ac.jp

Abstract—We have been carrying out a study on waveguide SIS mixers for large format multibeam receivers. The concept design was presented in ISSTT last year (Wenlei Shan, etc., “Concept Design of a Dual-Polarization Sideband-Separating Multi-Pixel SIS receiver,” ISSTT 2016). The main feature of this concept lies in the highly compact configuration with dual polarization receiving capability. The central part of the receiver is an integrated SIS mixer chip, on which planar orthomode transducers (OMTs) are formed on dielectric membranes. The LO introduced through metal waveguides is also coupled by membrane based probes. In this way, the metal waveguide network for LO distribution embedded in the mixer holder becomes much simpler and thus can be manufactured with conventional machining.

We have designed a single-pixel verification model operating in the 125 - 163 GHz band. This verification model incorporates all the necessary features that allow extending the design to an array. It is a dual-polarization and balanced mixer, and a sideband separation scheme will be fulfilled when a thin-film resistor process is established. We have fabricated membranes from SOI wafers with a deep reactive-ion etching process. Flat silicon membranes with 6-micrometer thickness have been fabricated in 3 mm x 3 mm windows. In this symposium, we are going to present the details of the circuit design and the fabrication process of the mixer chips.