

# TECHNOLOGY DEVELOPMENT FOR LONG WAVELENGTH ASTRONOMICAL SATELLITES

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**Abstract**— Here we present the characterization of the performance of a novel design for a digital spectrometer that could be used for high resolution cm/mm/submm spectroscopy. The CMOS ASIC spectrometer design, developed at JPL and UCLA, has dramatically lower power consumption than current approaches that generally employ Field Programmable Gate Arrays (FPGAs). Particularly for space missions and for small satellites, power consumption is a major issue. The order of magnitude lower power consumption of the ASIC approach is thus critical for future missions employing large-format focal plane arrays. Our task was to evaluate this 1024 channel, 1.3-GHz bandwidth CMOS spectrometer in terms of ability to integrate and its filter shape. The chip was to be tested largely at half-maximum speed to allow for use of the polyphase filter bank.

The results of this SURP show that the ASIC spectrometer can be made to perform largely as expected based on its design parameters. However, they suggest that more testing of the spectrometer chip is required. Based on the Allan Variance plots obtained, it is possible that there is an issue with the long-term integration of the chip; however, the reduced turnoff seems to indicate that while the output may have been drifting, the relative outputs between bins was drifting to a lesser extent. The filter shape testing confirms that the spectrometer has the resolution expected, and that its polyphase filter bank works properly. The higher noise floor for certain bins is something which could warrant investigation, but a -27dB noise floor is likely sufficiently low for the applications it will be used in. Finally, the anomalous filter shapes exhibited for a clock power level of -13dBm could be an artifact of the test system used, but warrant further investigation.