

## Planar-integration of Arrayed SIS Receiver Frontends

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**Abstract**—We have been conducting studies on planar integrated arrayed SIS receiver for wide field-of-view observation. Along with this study, our design ideas have gradually established, and were presented consecutively in previous ISSTTs (“Concept Design of a Dual-Polarization Sideband-Separating Multi-Pixel SIS Receiver,” ISSTT 2016; “Design and Fabrication of a Dual-Polarization,” ISSTT 2017). This approach has the following features: (1) independent coupling of signal and LO into a planar integrated mixer chip through membrane-based waveguide probes, (2) on-chip RF devices that include OMTs, hybrid bridges, and LO couplers, and (3) a much simplified LO metal waveguide distribution network that is embedded in the mixer mount.

For proof-of-concept, we have prototyped a single-pixel integrated SIS receiver, aiming to be readily extend to an array. The prototype receiver is designed at 2 mm wavelength to be capable of dual-polarization and balanced mixing. The mixer ICs are fabricated from silicon-on-insulator (SOI) wafers, which are locally thinned by a deep ion-etching process where LO and signal probes locate, with remaining silicon membranes of 6-micrometer thick. Orthogonally placed polarization-sensitive probes are adopted for signal coupling with polarization separation.

The mixer ICs were assessed in a 4 K cryostat. A corrugated feed horn is attached to the mixer mount for low cross-polarization signal coupling. The cross-polarization level of the horn/OMT combination was measured with a standard near-field beam scanner. Results of initial measurement show a cross-polarization level as low as -30 dB and a reasonable receiver noise. These results provide clear evidence of the feasibility of this planar integration approach.