

# Broadband Antireflective Silicon Optics for Terahertz instruments

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Submillimeter wave and THz instruments are central to contemporary astronomy, astrophysics, and cosmology research. Many applications from tens of GHz to THz frequencies, in ground and in space, would greatly benefit from large optics with broadband antireflective (AR) treatments. Silicon is a very interesting material at millimeter and submillimeter wavelengths. It has very low losses, even at ambient temperature, which makes it ideal for windows and optics, but its high refractive index ( $n_{Si} = 3.42$ ) makes AR treatment essential. Microfabrication of surface textures is an attractive technique for varying the effective refractive index of a material, thus, creating the AR structures [1]. Etching allows considerable flexibility in designing the texture geometry, which determines the effective index of refraction. Multilayers structures, where each layer is used to achieve a different index, can also be designed, providing a wider bandwidth compared to single-layer structures. Silicon Deep Reactive Ion Etching (DRIE) is used to individually pattern the wafers with posts or holes, of varying depth and width, calculated depending on the desired  $n$  index. The high resistivity wafers are then bonded together to produce the complete optic. Single-layer and double-layer designs have been simulated, fabricated and tested in the 190-330 GHz atmospheric window [2] with results showing less than -20 dB of reflectance over the full spectral band.

Building upon this work, we have simulated and fabricated a four-layer structure, with a 4:1 bandwidth, that is sufficient to cover the atmospheric windows at 125-170 GHz, 190-310 GHz and 335-355 GHz. As shown in Fig. 1, the two top layers T1 and T2 are posts with  $n$  index of 1.18 and 1.56 respectively. The two bottom layers T3 and T4 are holes with  $n$  index of 2.19 and 2.9 respectively. Using the DRIE process developed in [3], the two higher index layers (T3 and T4) are fabricated onto the same high resistivity wafer (W2), on the front and on the back. The second hole layer (T2) is fabricated on the backside of two additional wafers (W1 and W3). The 3 wafers (W1, W2 and W3) are then bonded together. After bonding, the lower index layer T1 is etched on the frontside and the backside of the stack. Fig. 1 presents Scanning Electron Microscope (SEM) images of the fabricated structures.

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Simulations show -20 dB of reflectance over all 3 atmospheric windows, measurement results are expected in the next few weeks and will be presented at the conference.

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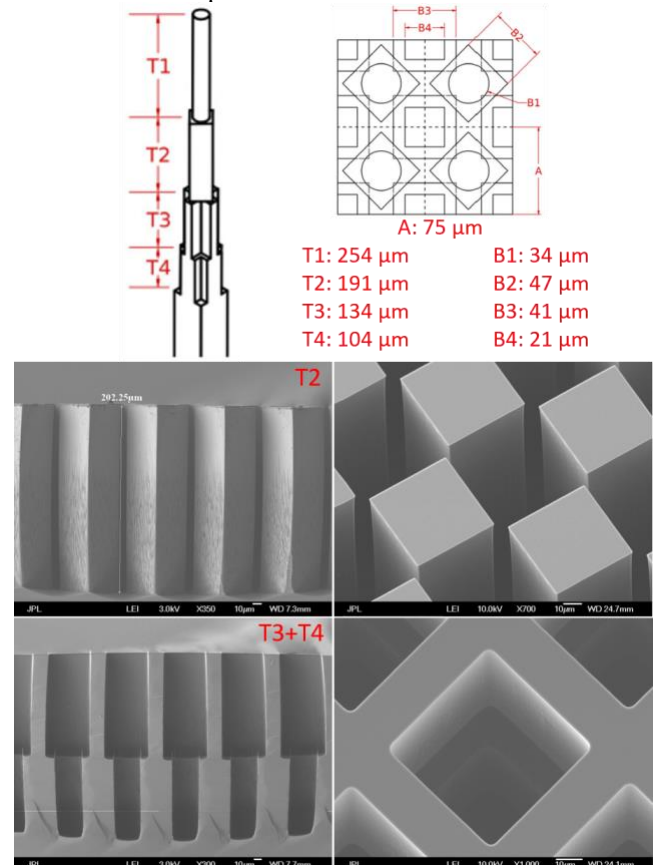


Figure 1: Schematic of the four-layer AR design with SEM images of the fabricated structures T2 and T3+T4, before bonding and etching of T1.

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