Electron Speed Saturation Effects in the Schottky Barrier Diodes Implemented in an 800 – 900 GHz Frequency Tripler

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***Abstract*— We report the manufacture and testing of a Schottky Barrier Diode (SBD) based frequency tripler able to handle more than 50 mW input power in the 270-300 GHz range with conversion efficiency of 5 %. The tripler integrates a single chip based on discrete SBD diodes developed at ACST. The electron speed saturation in the SBD semiconductor of this tripler can be achieved when increasing the input power. This effect significantly modifies the matching network of the tripler chip and induces strong deviations from expected results. The impact of this effect on the RF performance of the triplers is discussed and compared in this work.**

Keywords*— *Schottky, Tripler, Electron Speed Saturation

I. Introduction

The implementation of SBD technology for the development of mm-wave and submm-wave modules is a well know option to achieve compact and performant THz sources up to 2.7 THz [1]. SBD-based Frequency triplers are specially interesting to achieve the highest frequencies due to the larger multiplication factor and still reasonable conversion efficiency of up to ~5% at ~1 THz output frequency [2]. The SBD tripler technology developed at ACST can achieve at the moment 20%, 14%, 7% and 5 % at 300 GHz [3], 500 GHz [4], 700 GHz [3] and 900 GHz respectively. The tripler reported in this work uses the same discrete SBD technology described in [4], and it is based on the design architecture of the chip described in [5]. The available input power in WR3.4 for this tripler is much higher (70 mW) than it was possible to optimize for. This is due to the limitations in available space to fit a discrete diode for a 900 GHz tripler. The limitation of space in the chip limited this tripler to a maximum of 2 anodes, compared to other MMIC-based design able to fit even 4 anodes [5]. This tripler also achieved its best performance at an optimum input power of ~25 mW, but it can handle up to 50 mW without failure. The limitation in the number of anodes, the high frequency and the excessive available input power led us to find strong and clear electron speed saturation (ESS) effects in the semiconductor (SC) of the SBD. This is mainly due to the fact that the excessive input power excites a too large voltage amplitude response in the SBDs leading to a too fast voltage change. This effect is experimentally studied in this work and supported by simulations in EMpro/ADS softwares.

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II. Results

The experimental conversion efficiency of one tripler unit for two different levels of input power along its frequency band is plotted in Fig. 1. The solid lines represent a conversion efficiency (red) between 3-5% along the 800-900 GHz range when ~14 dBm input power is applied to the unit. Dashed lines illustrate the drop in conversion efficiency due to ESS when increasing the input power above 15 dBm. This tripler can be considered state-of-the-art in both high power and high efficiency compared to other ~900 GHz reported SBD triplers. The tripler reported in this work can match the similar output power achieved in [2] and [5] while only one chip is used (no power combining of chips) and having only two anodes in the chip instead of four [5]. The conversion efficiency in this work is twice larger than in [5] and as high as in [2] even if discrete SBD instead of MMIC approach.

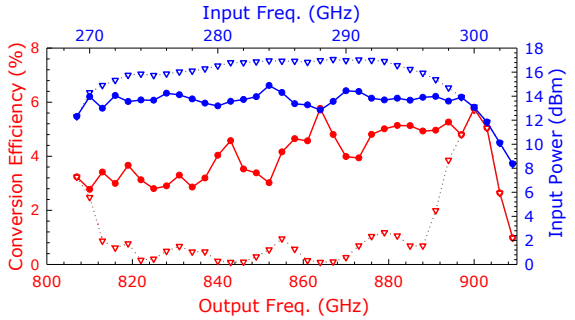

Fig. 1. Experimental efficiency (red) of the 800-900 GHz tripler with respect to the available input power (blue) in the 270-300 GHz range.

References

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