Preliminary Characterisation of a Compact 240 GHz SIS Dual-Polarisation Receiver for Large Array Applications

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***Abstract*—We report the development of an on-chip, compact dual-polarisation Superconductor-Insulator-Superconductor (SIS) receiver covering the millimetre frequency band from 190 GHz to 290 GHz. All the required components for the receiver are integrated on-chip using planar circuit technology, except the feedhorn. We use a 4-probe orthomode transducer (OMT) to couple the radio frequency (RF) and local oscillator (LO) and to split the incoming signal into two RF polarisation states before they are routed to the twin junction Nb/AlO$_x$/Nb mixers via a planar crossover, branch-line hybrids and bandpass filters. The entire receiver chip, only 4.0 mm by 4.1 mm in size, is mounted in a split block where the feedhorn and the magnetic biasing are located on the front side, and the intermediate frequency (IF) and DC biasing connectors are on the rear side, leaving the four adjacent sides of the block unobscured for a 2-dimensional extension into a multi-pixel array. In this paper, we present the receiver and mixer block design and preliminary experimental results obtained from testing the receiver.**

***Index Terms*—Heterodyne receiver, Superconductor-insulator-superconductor mixer, Dual-polarisation receiver, Focal Plane Array, Large format array;**

I. Introduction

Mapping large-scale structures in the Universe using heterodyne receivers, such as SIS mixers, requires long observation times due to the low pixel count in most instruments. Several multi-pixel focal-plane SIS arrays have already been developed, but most of these arrays only detect a single polarisation state of the incoming RF wave at a time [1]–[4].

The employment of single-polarisation receivers results not only in the loss of the polarimetry information but also in the loss of sensitivity since we are only detecting half of the incident signal power. Therefore, dual-polarisation receivers are favourable for their astronomical observation capabilities. However, most dual-polarisation receivers deployed to date are primarily a stack of two single-polarisation receivers with a waveguide OMT or a free-space optical element to separate the polarisation information [5]–[8]. The receiver setup, therefore, requires additional space, which does not provide a compact layout required for array extensions.

Here, we present a compact on-chip dual-polarisation receiver, which can be easily scaled to higher frequencies, as well as to form a large dual-polarisation heterodyne array. All the required RF components are fabricated on a single quartz chip using planar superconducting circuit technology.

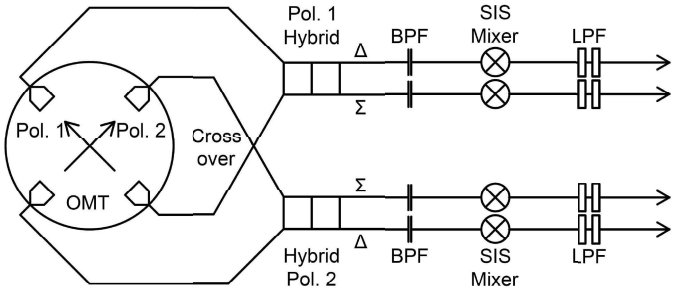

Fig. 1. A schematic of the receiver chip.

Consequently, the mixer chip can be housed in a split-block without any waveguide structure, apart from the feedhorn, which is drilled directly into the copper block, using the smooth-walled horn technology [9], [10].

II. The Dual-Polarisation Receiver Design

A detailed description of the receiver design has already been reported [11]. Hence, below, we will only give a brief account of the receiver design. Fig. 1 shows a schematic of the dual-polarisation receiver chip. A picture of the receiver chip is shown in Fig. 2. The receiver has all the front-end elements fabricated onto a single quartz chip and connected with microstrip transmission lines. A 4-probe OMT using two sets of opposing probes in a circular waveguide is used to split the LO and RF power incident at the feed horn into two orthogonal polarisations. The signals from each probe set, coupling one polarisation state, are then recombined at the quadrature hybrid Σ output port.

The microstrips connecting the OMT probes and the hybrids inevitably result in crossing transmission lines, which connect to OMT probes that couple different polarisations, as shown in Fig. 1. The crossover must be designed to minimise crosstalk between the two polarisations. Instead of interconnecting the microstrips in the wiring layer, a short coplanar waveguide (CPW) section is deposited in a gap in the ground layer where the Pol. 1 signal is routed underneath the Pol. 2 microstrip, as shown in Fig. 3. The CPW in the ground layer is capacitively connected to the feeding microstrip via broadside couplers, allowing for a closed dielectric layer throughout the chip. In summary, the crossover allows to connect the

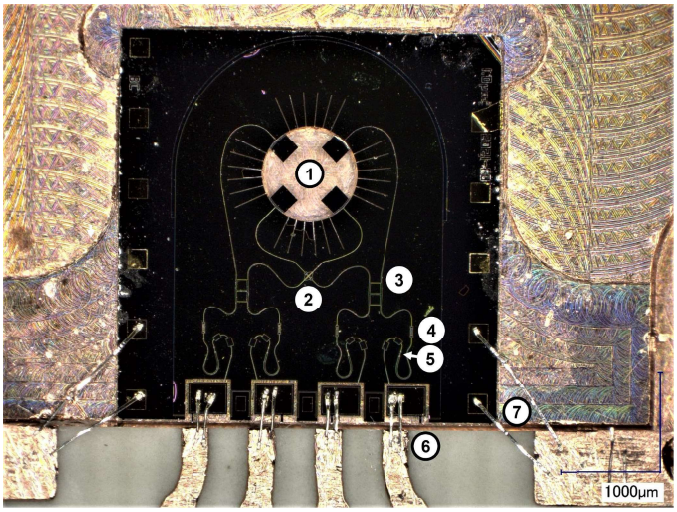

Fig. 2. The thinned receiver chip mounted in the bottom block and bonded to the IF transformer. The chip consists of the OMT (1), the crossover (2) and two hybrids, where the hybrid for Pol. 1 is marked with (3). All hybrid outputs connect via a BPF (4) to a twin junction SIS mixer (5), which connects via the LPF and bond wires to the IF transformer (6). The ground is connected at (7).

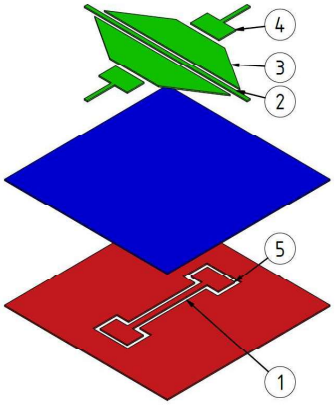

Fig. 3. An explosion view of the microstrip layers at the crossover. The ground plane is shown in red, the dielectric layer in blue and the wiring layer in green. Pol. 1 is routed in a CPW in the ground plane (1) underneath the Pol. 2 microstrip (2), which is bracketed to form a CPW in the wiring layer with two conductor patches (3). The Pol. 1 signal is connected via broadside couplers in the wiring layer (4) and the ground plane (5).

OMT probes to the hybrids for the respective polarisations to recombine the signals of each polarisation splitting between each probe set.

The hybrid has two outputs, the Σ output port containing the full strength of one of the polarised signals and the isolated Δ output. Both hybrid output ports connect to two identical mixer circuits for impedance symmetry reasons, although the Δ mixer circuit should couple only noise and can be terminated. The mixer circuits comprise a bandpass filter (BPF), a twin junction SIS mixer and a lowpass filter (LPF). The BPF is used before the SIS mixer to provide separate DC biasing and block the IF signal. The LPF after the mixer prevents RF signal leaking into the IF circuitry and ensures efficient RF coupling to the SIS junctions. The SIS mixer comprises two identical tunnel junctions in a conventional twin junction

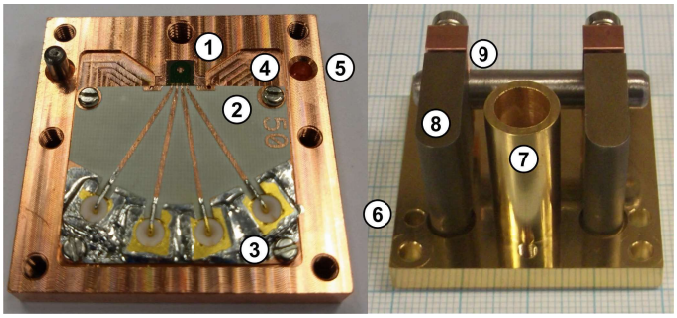

Fig. 4. The receiver is made from the bottom block on the left, the top block on the right, and the receiver chip on a pedestal in the bottom block (1). The receiver chip is wire bonded to the IF transformer (2), which ends in SMP connectors (3) to the back of the receiver. The bottom block has a recess for the IF transformer and coil shoes (4). An identically shaped but deeper counterpart is in the top block. Dowel holes in the bottom (5) and top (6) block align the feedhorn (7) with the receiver chip and the backshort section, which is milled into the bottom block. The magnetic assembly consists of a feed (8) connecting the shoes next to the receiver chip with the coil, which sits on a rod clamped on the feed (9).

arrangement to tune out the junction capacitance and maximise the coupling of power to the SIS mixer. As the mixer circuits are used to impedance match the Δ hybrid ports for both polarisations, each receiver chip contains eight SIS devices in four twin junction circuits.

Each on-chip circuit element is initially designed independently using the 3D electromagnetic software Ansys HFSS before interconnecting them with microstrip transmission lines to form the entire receiver chip. The full chip design is then carefully tweaked and optimised for bandwidth, identical power coupling between the two polarisation states, and minimised transmission losses. The detailed design description is published in [11].

The entire receiver is fabricated onto a 4.0 mm by 4.1 mm quartz substrate, hence the design of our split block is substantially simplified. As shown in Fig. 4, the mixer block is made up of two separate parts without the need for any complicated mechanical structure. The top block comprises a compact drilled horn and openings for the magnetic circuit assembly, and the bottom block has a large area milled out for hosting the mixer chip, magnetic shoes, and IF transformer with holes for the IF and DC connectors. The entire mixer block is only 40 mm by 40 mm, the size determined primarily by the size of the IF SMP connectors and the IF transformer. It is worthwhile noting that the block has plenty of space to accommodate different sizes of IF circuitries and magnetic bias options, so the block size can be further reduced if necessary.

The receiver is mounted in the cryostat and connected to the signal processing chain, as shown in Fig. 5. The four mixer circuits on the receiver chip connect via SMP connectors to the SMA connectors of the bias tees. SMP connectors are used due to the smaller footprint of the push-pull mechanism in comparison to the hex nut, which would need additional space for a spanner, keeping the receiver compact. The two bias tees connected to the Σ mixer circuits connect to circulators and low noise amplifiers to route the IF signal to room temperature, while the two bias tees connected to the Δ mixer circuits have terminated AC ports. The DC ports of the four bias

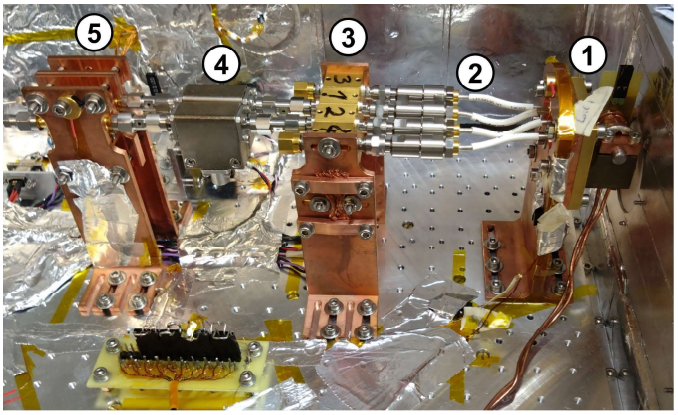

Fig. 5. The cryostat setup. The receiver (1) is connected via four SMP-to-SMA cables (2) to four bias tees (3). The outer two bias tees are terminated as they connect to Δ twin junctions, and the inner two bias tees connect via two isolators (4) and low noise amplifiers (5) to room temperature.

TABLE I
THE 5-STEP PLANAR-CIRCUIT THIN-FILM DEPOSITION PROCESS.

Step	Description	Material	Thickness
1	Deposition trilayer	Nb/AlO_x/Nb	400/1/200 nm
2	Etching junctions from trilayer	Nb Remains	400 nm
	Deposition of first dielectric	SiO	200 nm
3	Deposition of second dielectric	SiO	200 nm
4	Deposition of wiring layer	Nb	400 nm
5	Deposition of bonding pads	Ti/Au	10/150 nm

tees connect independently to room-temperature four-way bias modules and a data acquisition unit. Thus, the DC signal of all four mixers can be swept and read simultaneously. The linear arrangement of the signal processing chain behind and within the footprint of the receiver can be extended to an array in an ALMA-style cartridge.

III. Receiver Fabrication

The planar receiver chip is fabricated at the facilities of the Observatoire de Paris with a 5-step recipe, summarised in Table I. In the first step, the ground plane conductor is sputtered on the substrate in the form of a 14 kA/cm^2 Nb/AlO_x/Nb trilayer, except for areas at the OMT, the IF bonding pads and CPW features of the crossover and BPF. The top layer of the trilayer is removed by reactive ion etching (RIE) in the second step and replaced with a first 200 nm SiO layer, except at the SIS junction locations. Thus, the area of the SIS junctions is defined, the top and bottom electrodes of the SIS junction are isolated by AlO_x and the remaining ground plane covered with SiO. A second 200 nm SiO layer is evaporated on the substrate in the third fabrication step to achieve the desired characteristic impedances and to minimise the likelihood of shorts between the ground conductor and the wiring layer. The second SiO layer leaves a 6 µm^2 window around each SIS junction with only 200 nm SiO to ensure contact between the trilayer top electrode and the wiring layer. The wiring layer is sputtered in the fourth fabrication step. The last deposition step is the evaporation of Ti and Au on areas used for wire bonding.

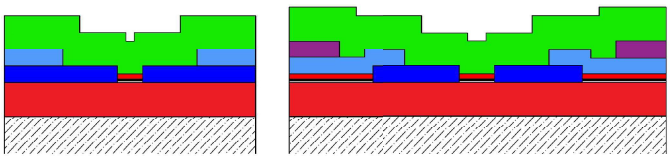

Fig. 6. Side views of the original mask set (left) and of the revised mask set (right) with larger SIS junctions and an additional SiO layer; The quartz substrate is shown hashed. The Nb of the trilayer is shown in red, which sandwiches the passivated Al in white and black. The first SiO layer is deposited where the trilayer has been removed, shown as dark blue. The second SiO layer is pale blue, and the third SiO layer is purple. The wiring layer Nb is shown in green.

A. DC Characterisation

After dicing the wafer and before thinning the receiver substrate to the thickness required for RF testing, we conducted DC screening tests. We have four device variations with junction areas of 1.0 µm^2 or 1.5 µm^2.

The DC screening results of the first fabricated batches showed a low fabrication yield, which is not unexpected, but too small for our devices requiring eight functioning SIS junctions. Consequently, we reviewed the recipe by also fabricating separate test device batches with 1.0 µm^2 to 10 µm^2 SIS junctions, and we found evidence that the large ground layer of our receiver causes issues during the RIE process. We suspect that the SF_6 etching of the trilayer might have polluted the photoresist defining the SIS junction area, preventing a clean lift-off. In the deposition of the wiring layer, these photoresist remnants were then sandwiched between the SIS top electrode and the wiring layer, causing a resistive response.

Accordingly, we modified the fabrication process by 1) increasing the SIS junction area and 2) reducing the area etched to define the SIS junctions. The mask of the second fabrication step now has a larger SIS junction area but only exposes the trilayer at a 10 µm^2 square around the SIS junctions to the RIE and subsequent SiO deposition, as shown in Fig. 6. Hence, the ground layer at most of the receiver chip consists of the trilayer, which is covered with 200 nm SiO and a 6 µm^2 square around the SIS junctions in the third fabrication step. An additional (3.5) fabrication step is inserted before the fourth step of Table I to deposit another 200 nm SiO with a 14 µm^2 square around the SIS junctions to achieve 400 nm SiO on most of the chip and, therefore, the desired characteristic impedances. With these modifications, the fabrication yield improved significantly.

The increased junction size inevitably affected the performance of the receiver. As shown in Fig. 7, the return loss of a signal incident at the circular waveguide is very high, but the ripples reach below –10 dB up to 240 GHz, offering us a chance to characterise the on-chip integrated circuit. In the initial design, most of the incident signal couples in the second SIS junction. Our simulation showed that the increased junction area causes the incident signal to couple mostly into the first SIS junction of the twin junction, leaving the second SIS junction with very little coupling. Despite this change, the total coupling in both SIS junctions is similar to that of the initial design at low RF frequencies.

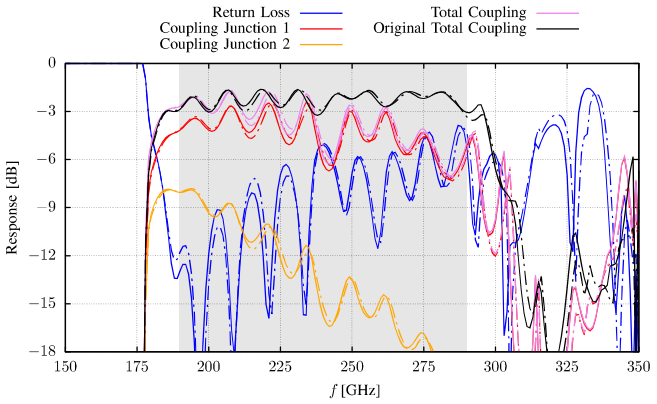

Fig. 7. The simulated overall performance of the receiver chip fabricated with the revised mask set and 3.0 µm^2 SIS junctions. The Pol. 1 responses incident at the circular waveguide of the model are shown as solid lines, and Pol. 2 responses as dash-dotted lines. Total coupling denotes the sum over the two SIS junctions of a twin junction circuit.

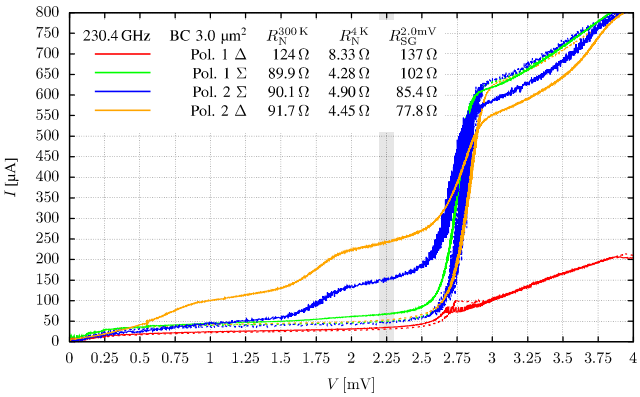

Fig. 8. The pumped IV curves and the unpumped IV curves (dotted) of the four twin junction circuits. The legend summarises the 300 K resistance, the normal resistance at 4 K and the subgap resistance measured at 2.0 mV. The grey shaded area is the (2.25 ± 0.05) mV interval used to gauge the direct detector response to the LO signal.

B. Receiver Preparation

We selected devices for thinning to the designed quartz thickness of 50 µm based on the fabrication yield measured by sampling devices across the wafer. The devices were thinned with a dicing saw at the Rutherford Appleton Laboratory. The thinned devices were mounted with a brush to their position in the bottom block and affixed with agar scientific ltd crystalbond 555, a low melting point (54°C) adhesive. Crystal bond is more versatile than the commonly used superglue since it can be applied without time restrictions and re-liquefied for adjustments.

A frequent source of difficulty was applying pressure on the receiver chip to remove excess adhesive between the chip and the bottom block. The excess adhesive would elevate the chip and consequently cause the chip to touch the top block, potentially destroying the receiver chip once assembling the receiver. In case the receiver chip protruded from the bottom block, we liquefied the crystal bond and adjusted the chip position. We followed the same procedure when we could identify an imperfect alignment of the backshort section underneath the transparent OMT. Once the receiver chip mounting in the bottom block was satisfactory, the receiver chip was wire-bonded to the IF transformer, and then the top block was mounted on the bottom block, forming the receiver. The receiver was mounted in the cryostat for RF characterisation.

IV. Optical Coupling Characterisation

The optical coupling of the receiver was tested using the twin junctions as direct detectors, with an LO source directly facing the receiver in the cryostat behind a Zotefoam vacuum window and a Zitex IR filter. The photon-step responses of the four twin junctions enabled us to infer the coupling efficiency of the circuit, particularly from the circular waveguide to the microstrips at the OMT and the power-combining capabilities of the hybrid.

The first thinned device we characterised has 3 µm^2 SIS junctions and has not been screened before thinning. The corresponding IV responses and parameters are shown in Fig. 8. The 300 K resistance test showed that the warm resistance of the Pol. 1 Δ twin junction has a resistance of 124 Ω, indicating that the twin junction device is faulty. The faulty response can be seen from the unpumped response with very low tunnelling current at the gap voltage, potentially caused by a defective SIS junction and a series resistance.

A. Power Measurement

The pumped IV responses in Fig. 8 show the highest photon step current we could achieve at 230.4 GHz, although the Gunn LO source was directly illuminating the horn, hence should have been strong enough to saturate the IV response. We conclude that the coupling of the SIS junctions to the LO source is poor, either due to faulty subcircuits or excessive losses. Furthermore, the LO couples to both twin junctions connected to the Pol. 2 hybrid. However, despite that the Δ twin junction was designed to be isolated, more LO signal couples to the Δ twin junction than the Σ twin junction at 230.4 GHz. In contrast, both twin junctions connected to the Pol. 1 hybrid are not at all responding to the LO. Following the design, a photon step should appear in the Pol. 1 Σ twin junction, considering that it has a good unpumped IV response. However, as the Δ twin junction is defective, we can not extract information to learn if any LO signal is incident at the Pol. 1 hybrid.

Fig. 9 shows the photon step current at a bias voltage centred at 2.25 mV as a function of LO frequencies. The data comprises two different cooldowns, a preliminary test and one cooldown designated for this frequency sweep, where most data points were recorded by sweeping the LO frequency. Photon steps appear in both twin junctions connected to the Pol. 2 hybrid at all frequencies. Since the power in the Δ and Σ ports are approximately equal, the observed behaviour resembles a single input signal into the hybrid, splitting with −3 dB and 90° phase difference between the outputs.

B. Polarisation Measurement

In order to confirm that the photon step responses in the Σ and Δ twin junction of the Pol. 2 hybrid originate from

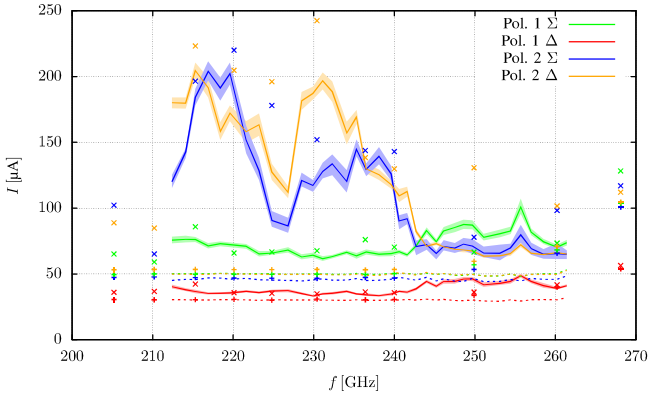

Fig. 9. The current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ at various LO frequencies. The unpumped currents are shown as dotted lines. $\times$ and $+$ show the pumped and unpumped data of the same experiment taken in a preliminary test.

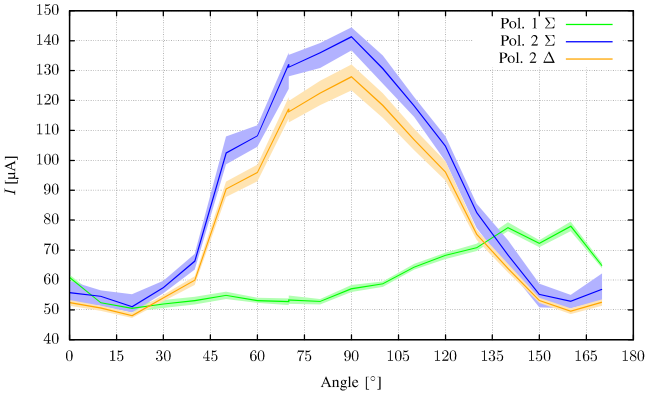

Fig. 10. The current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ at different orientations of the wire grid at 216.8 GHz.

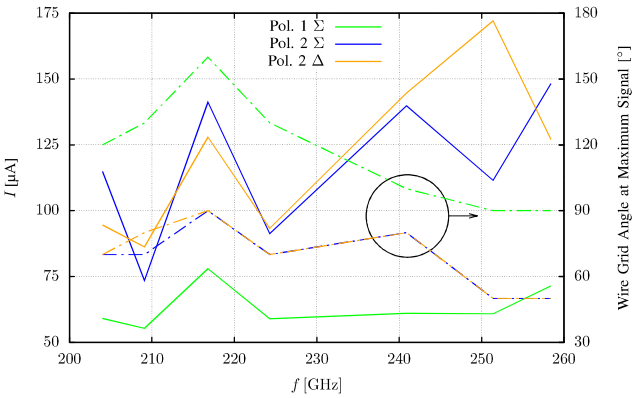

Fig. 11. The maximum current of the pumped IV curve at a bias voltage of $(2.25 \pm 0.05)\,\mathrm{mV}$ in solid lines and the corresponding wire grid orientations in dash-dotted lines at various LO frequencies.

the same signal polarisation, we change the LO polarisation. Instead of rotating the LO source, we placed a wire grid between the LO source and the vacuum window. This reduces uncertainties and difficulties associated with the optical alignment as the LO source and wire grid are positioned only once. However, this method inevitably introduces losses due to the addition of the wire grid in the optical path.

The photon step currents centred at 2.25 mV are shown in Fig. 10 as a function of the wire grid orientation. We again recorded different LO powers for each data point and stepped the wire grid orientation by 20° to interleaf the data of a full rotation to the shown 10° resolution.

Both twin junctions attached to the Pol. 2 hybrid show photon-step currents varying sinusoidally with the wire grid angle and peaking together. This observation implies that the Σ and Δ twin junction responses originate from the same LO polarisation. Furthermore, since the power in the Δ and Σ ports is almost equal, it raises the possibility that the LO power is injected at only one hybrid input.

The current into the twin junction attached to the Pol. 1 hybrid Σ port is significantly less at the peak of the Pol. 2 photon step response compared to its maximum current. The peak of the Pol. 1 Σ twin junction occurs at a wire grid angle of 150°, providing evidence that the OMT, indeed, splits the two polarisations. However, the wire grid angles corresponding to the two polarisation peaks differ by only approximately 60°. This angle, however, was designed to be 90°, indicating some issues with the polarisation splitting capabilities of the OMT. Again, this observation is with the caveat of a defective Pol. 1 Δ twin junction.

We repeated this experiment for a set of LO frequencies shown in Fig. 11. Throughout, we observe that the photon steps of Pol. 1 and Pol. 2 peak at wire grid angle differences well below 90°. In spite of this discrepancy, the photon step currents of the two Pol. 2 twin junctions peaked at the same grid angle at all frequencies. An interesting observation is that the photon step currents peaked at different angles depending on the LO frequency. A reaffirming observation is that the photon step response varies sinusoidally with a period of 180°, indicating that the experimental setup is fine.

C. Summary of RF Testing

We can summarise the RF testing in the previous section as follows: We have had difficulties pumping the twin junctions and were unable to saturate them at any frequency, although the Gunn LO has been facing the receiver directly. The characterisation of Pol. 1 has been compromised by the defective twin junction attached to the Pol. 1 Δ hybrid output. The Pol. 1 Δ twin junction response has been negligible throughout, and the Pol. 1 Σ twin junction response has shown rather small photon steps. In contrast, both twin junctions attached to the Pol. 2 hybrid showed clear photon steps. For Pol. 2, it depends on the LO frequency, which twin junction circuit, Σ or Δ, shows the larger photon step current. We confirmed that the responses of the twin junction circuits attached to the Pol. 2 hybrid originate from the same polarisation by rotating a wire grid inserted between the LO source and the cryostat vacuum window.

The optical coupling characterisation reveals two issues with the device:

1) The coupling of LO power from the Gunn LO source to the twin junctions is weak.

2) Both twin junctions attached to the Pol. 2 hybrid respond similarly to the LO with frequency dependence.

V. Investigation of the Causes for Weak Coupling

The weak coupling of LO power of the receiver could be caused by several factors, including:

1) Misalignment in assembling the top and bottom split blocks, where the feedhorn and OMT were aligned. This causes the waveguide containing the four OMT probes in the bottom block to be displaced with respect to the feeding circular waveguide in the top block. To investigate the influence of the displacement on the coupling, we simulated the behaviour with Ansys HFSS. The results are shown in Fig. 12, where we assumed that there is a misalignment of 10% of the waveguide diameter along the axis of a particular polarisation. The OMT probe shifting away from the circular waveguide couples significantly less than the opposing OMT probe, which shifts towards the centre of the circular waveguide. We also observe some cross-coupling into the OMT probes of the orthogonal polarisation. However, the coupling to this polarisation is affected very little by this misalignment.
   These simulations demonstrate that a displacement of the two circular waveguides could account for the poor coupling experienced in the experiment.
2) Fabrication defects of the receiver components on the chip. The on-chip receiver contains several components that require skilful fabrication for the receiver to operate as designed. We, therefore, inspected the receiver chip under the microscope and found the following:
   The crossover: The visual inspection showed that the transmission lines comprising the crossover are clean, and, therefore, assuming that no short to the ground plane exists, we don't expect the weak coupling to be caused by the crossover component.
   The hybrid: The transmission lines comprising the hybrids looked to be in good shape. Again, we expect the poor coupling to be caused by the hybrid fabrication. It is interesting, however, to emphasise that the Σ and Δ ports of Pol. 2 received the same amount of power as our test in the previous section demonstrated.
   The BPF: Inspection of the BPF under the microscope does show small defects in fabrication that could cause shorts to ground in both mixer circuits attached to the Pol. 2 hybrid, which could explain the weak coupling.

In order to find out the main reason for the poor coupling that we are experiencing, we are planning to perform the following experiments:

- Removing the wire grid and altering the polarisation by rotating the LO source. So far, we assumed that the LO power emitted from a rectangular waveguide and drilled feedhorn is polarised in an orientation that pumps each receiver polarisation with approximately 50% because our OMT probes are oriented by 45° with respect to the rectangular waveguide. Rotating the LO source, and therefore its rectangular waveguide, allows us to modify the coupling to the two sets of probes and will hopefully shed more light on the receiver behaviour.
- Removing the three horizontal connections of the hybrids, shown in Fig. 2. Each OMT probe will then connect to a twin junction circuit directly, allowing us to measure which OMT probe couples LO power. It will then also remove any potential problem in the hybrid design.
- Optical verification of the alignment of the top and bottom blocks, which could cause the displacement of the circular waveguide in the bottom block to the waveguide in the top block.

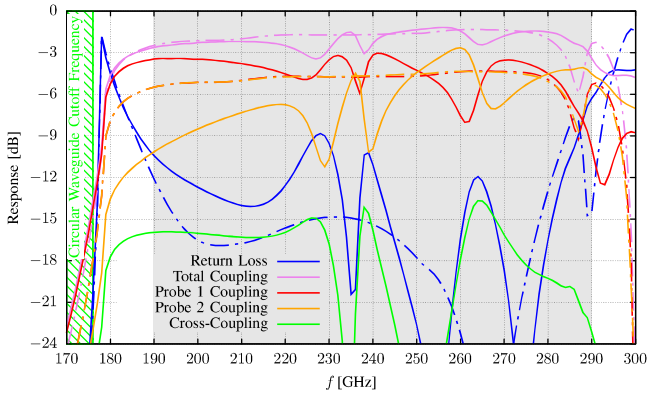

Fig. 12. The simulated OMT performance with the circular waveguide offset by 100 µm towards Probe 2 of the polarisation, which responses are shown as solid lines. The orthogonal polarisation, shown dash-dotted, shows largely similar responses to the designed performance, especially below 270 GHz, except for the excess cross-coupling in green.

VI. Conclusion

We have investigated the performance of an on-chip compact dual-polarisation receiver using SIS tunnel junctions in the frequency range of 190 GHz to 290 GHz. Our experimental test showed weak coupling to the SIS junctions, and we thoroughly experimentally investigated the polarisation behaviour of the receiver and concluded that the most likely reason for the poor coupling comes from a misalignment of the circular waveguide containing the four probes to the waveguide feeding the LO power. Further investigations are in progress to confirm the reason for poor coupling, including the employment of a different split block.

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REFERENCES

[1] H. Smith, J. Buckle, R. Hills, G. Bell, J. Richer, E. Curtis, S. Withington, J. Leech, R. Williamson, W. Dent, P. Hastings, R. Redman, B. Wooff, K. Yeung, P. Friberg, C. Walther, R. Kackley, T. Jenness, R. Tilanus, J. Dempsey, M. Kroug, T. Zijlstra, and T. M. Klapwijk, "HARP: a submillimetre heterodyne array receiver operating on the James Clerk Maxwell Telescope," in *Millimeter and Submillimeter Detectors and Instrumentation for Astronomy IV*, 2008.

[2] C. Groppi, C. Walker, C. Kulesa, D. Golish, J. Kloosterman, S. Weinreb, G. Jones, J. Barden, H. Mani, and T. Kuiper, "SuperCam: A 64 pixel heterodyne array receiver for the 350 GHz atmospheric window," in *20th Int. Space Terahertz Technol. Symp*, 2009, pp. 90–96.

[3] C. E. Groppi and J. H. Kawamura, "Coherent detector arrays for terahertz astrophysics applications," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 85–96, 2011.

[4] J. Garrett, J. Leech, F. Boussaha, C. Chaumont, B. Ellison, and G. Yassin, "A 1x4 focal plane array using 230 GHz SIS mixers," in *2018 29th IEEE International Symposium on Space Terahertz Technology, ISSTT 2018*, 2018.

[5] R. Guesten, G. A. Ediss, F. Gueth, K. H. Gundlach, H. Hauschildt, C. Kasemann, T. Klein, J. W. Kooi, A. Korn, and I. Kramer, "CHAMP: The carbon heterodyne array of the MPIfR," in *Advanced Technology MMW, Radio, and Terahertz Telescopes*, vol. 3357. SPIE, 1998, pp. 167–177.

[6] K. F. Schuster *et al.*, "A 230 GHz heterodyne receiver array for the IRAM 30 m telescope," *Astronomy and Astrophysics*, 2004.

[7] V. Belitsky, I. Lapkin, B. Billade, E. Sundin, A. Pavolotsky, D. Meledin, V. Desmaris, M. Strandberg, R. Finger, and O. Nyström, "Prototype ALMA Band 5 Cartridge: Design and Performance," in *Proc. 20th Intl. Symp. Space Terahertz Tech*, 2009, pp. 2–5.

[8] J.-Y. Chenu, A. Navarrini, Y. Bortolotti, G. Butin, A. L. Fontana, S. Mahieu, D. Maier, F. Mattiocco, P. Serres, and M. Berton, "The front-end of the NOEMA interferometer," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 2, pp. 223–237, 2016.

[9] P. Kittara, A. Jiralucksanawong, G. Yassin, S. Wangsuya, and J. Leech, "The design of potter horns for THz applications using a genetic algorithm," *International Journal of Infrared and Millimeter Waves*, vol. 28, no. 12, pp. 1103–1114, 2007.

[10] J. Leech, B. K. Tan, G. Yassin, P. Kittara, and S. Wangsuya, "Experimental investigation of a low-cost, high performance focal-plane horn array," *IEEE Transactions on Terahertz Science and Technology*, vol. 2, no. 1, pp. 61–70, 2011.

[11] J. Wenninger, F. Boussaha, C. Chaumont, B. K. Tan, and G. Yassin, "Design of a 240 GHz On-Chip Dual-Polarization Receiver for SIS Mixer Arrays," *Superconductor Science and Technology*, 2023.