

Exploring the Limits of the Tunnel Junction Fabrication Technique for Josephson Junctions TWPA and the Preliminary Characterisation Results

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Abstract— Travelling Wave Parametric Amplifiers (TWPAs) can potentially achieve quantum limited noise over a broad bandwidth in the microwave regime, with potential applications in the readout of millimetre (mm) and sub-millimetre (sub-mm) receivers to further improve the system sensitivity, among many other applications. TWPAs using embedded Josephson junctions (J-TWPA) have proven to exhibit noise performance approaching the quantum limit, however its compression point ($P_{-1dB} \sim -100$ dBm) is too low for reading out mm and sub-mm astronomical receivers. Therefore, we explored the design of higher dynamic range JTWPAs to match the power requirements, and to optimise the performances of the JTWPA for this specific application. Our aim is to adapt the well-established Nb-AlO_x-Nb tri-layer fabrication technique used routinely for developing high-quality Superconductor-Insulator-Superconductor (SIS) tunnel junctions to fabricate our JTWPA. Therefore, we present in this paper our investigation of the feasibility of such technique in fabricating large number of lower critical current density junctions embedded in a coplanar waveguide (CPW). The preliminary results on a 500-junctions device are in line with the expected behaviour, showing a measured gain consistent with theoretical calculations which demonstrates the potential use of the tri-layer tunnel junction technology for the fabrication of JTWPAs.

Keywords—travelling waves, parametric amplifier, quantum limited, Josephson junctions, critical current density

I. INTRODUCTION

The travelling wave parametric amplifier (TWPA) is an emerging technology capable to achieve broadband high gain in the microwave regime with quantum limited noise performance. These appealing characteristics derive from the use of reactive properties of a superconducting transmission line formed using either high kinetic inductance superconducting film (KI-TWPAs) [1] or embedded Josephson junctions (J-TWPAs) [2], to transfer energy from a high amplitude pump tone to a weak signal. TWPAs may find applications in many fields ranging from quantum computing [3], dark matter axion search [4,5] to astrophysics, where it could replace the semiconductor-based readout amplifiers on millimetre (mm) and sub-millimetre (sub-mm) telescopes to decrease power dissipation and enhance the overall signal to noise ratio [6].

For applications requiring high power handling capability, including the readout of mm and sub-mm receivers' down-converted IF signal, KITWPAs are often preferred due to their higher compression point (-60 dBm $< P_{-1dB} < -40$ dBm). However, it requires long transmission lines and high pump powers, which may increase heating and induce Johnson noise, hence compromising the noise performance. On the contrary,

JTWPAs have high inductance per unit length, therefore requiring shorter transmission lines and lower pump power to achieve similar high gain. Nevertheless, these advantages come at the cost of a lower compression point ($P_{-1dB} \sim -100$ dBm), restraining its application as readout for mm and sub-mm receivers beyond -100 dBm compression point.

The characteristic of a JTWPAs, including the dynamic range or power handling capability, is dictated by the various parameters of the “unit cell” (see Fig.1) comprising one or several Josephson junctions (JJs) embedded within a small section of the transmission line that is subsequently cascaded to form the amplifier. As the properties of the JJ can be easier to control compared to searching and fabricating exotic superconducting material in the case of KITWPAs, we opt to explore the possibility for engineering the behaviour of JTWPAs to realise a quantum amplifier that could match the power requirements of mm and sub-mm receivers (-90 dBm $< P_{-1dB} < -80$ dBm), while retaining the quantum-limit noise performance.

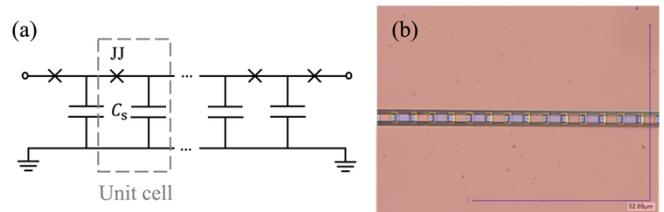


Figure 1. A unit cell cascaded repeatedly to form a full JTWPA. (a) Circuit diagram illustrating the unit cell where the cross represents the Josephson junction and C_s is the shunt capacitance to ground of the transmission line. (b) Optical microscope's image of a test device using false colours to identify the silicon substrate (grey), first niobium metallisation layer (red), SiO₂ dielectric layer (yellow), the Josephson junction (blue) and the second niobium metallisation layer (purple).

II. TEST DEVICES

A high gain JTWPA requires high inductance per unit length, which translates to the need for low critical current junctions around $J_c < 0.3$ kA/cm² with small area (< 1 μm²). This need for low critical current junction is in fact in contrast to the aim of Superconductor-Insulator-Superconductor (SIS) junctions' fabrication which often attempt to reach as high a J_c as possible. Given that the SIS fabrication procedure has been refined over many years of research and is more accessible for the astronomical community, we therefore intent to explore the know-how of such fabrication technique to engineer the junction properties that would suit to our objective. Furthermore, this opens up the opportunity to integrate the

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JTWPA with the mm/sub-mm detectors in the near future e.g., fabricating the SIS mixer and the JTWPA on to a single chip using the same junction technology.

In order to understand how we can alter the well-established SIS junction fabrication recipe to realise the junction characteristic we need, i.e., larger number of junctions with low critical current density; we designed and fabricated test devices with 100, and 500 Nb-AlO_x-Nb junctions embedded in series within a niobium coplanar waveguide (Fig.1(b)). These devices are fabricated using four photolithography steps and an additional e-beam lithography step to define the junctions with different sizes ($A_{JJ} = 0.25, 0.5$ and $1 \mu\text{m}^2$). We fabricate three sets of devices using 280- μm thick high-resistivity silicon wafers; and we altered the tri-layer deposition parameters for each set of devices to assess the junction's critical current density. The resulting measured J_c values (4, 3.5 and 2.5 kA/cm²) as a function of the oxygen exposure $E = P_{O_2} \cdot t$, where P_{O_2} is oxygen partial pressure and t is oxidation time, are plotted in Fig.2; together with previous measurements at the same fabrication facilities (red dots) and data provided by our collaborators at GEPI, Observatoire de Paris (blue dots). The results clearly expose a $J_c(E)$ dependence proportional to $E^{-\beta}$, where the calculated $\beta = 0.4$ is consistent with results previously published in the literature [7].

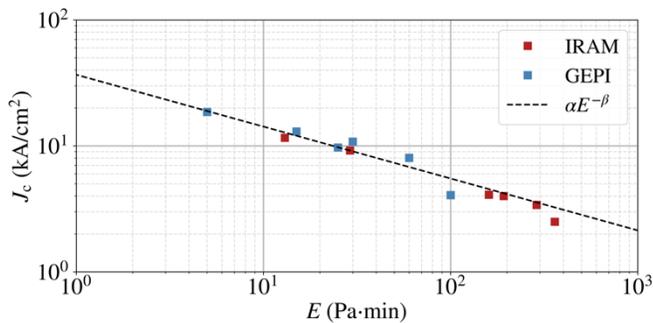


Figure 2. Measured critical current density J_c values as a function of the oxygen exposure E during the tri-layer fabrication process. The red dots with $J_c = 4, 3.5$ and 2.5 kA/cm^2 correspond to the set of devices fabricated at the Institut de Radioastronomie Millimetrique (IRAM) for this project; further data from previous fabrication rounds have been added to better estimate the trend. The blue dots correspond to data from our collaborators at GEPI, Observatoire de Paris. We measure a $J_c(E)$ dependence, where $\alpha = 36.8$ and $\beta = 0.4$.

III. EXPERIMENTAL SETUP

We performed the DC and the RF characterisation of our devices at cryogenic temperatures (4K) to investigate the yield and accuracy of our refined fabrication recipe. First, we prepared the samples by mounting the chip on top of a cooper PCB board made using 2-mils thick Roger Duroid RO4350b material, patterned with a straight 50 Ω CPW line, except the area where the chip will be placed. The chip is bonded with aluminium bond-wires to make the electrical connections between the PCB and the chip, as shown in Fig.3(a). The PCB is then placed in a sample holder, as shown in Fig.3(b), and attached to a cooper bracket anchored to the cold plate of a 4K cryostat system.

The experimental setup inside the cryostat is displayed in Fig.4. We use a combination of a four-way splitter and a four-channels switch to measure up to 3 devices in a single cool-down. The DC characterisations were performed using a DC current source and a voltmeter, conducting a four-wire

measurement of the chip using bias-tees on the RF lines. For the RF characterisation, we use a vector network analyser (VNA), and we calibrate the RF transmission measurement with a blank PCB sample inside the cryostat.

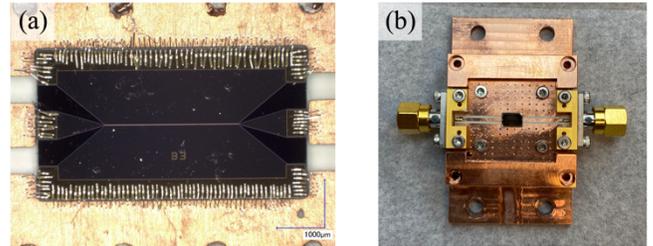


Figure 3. (a) Test device mounted and bonded to the PCB. (b) PCB mounted in the sample holder.

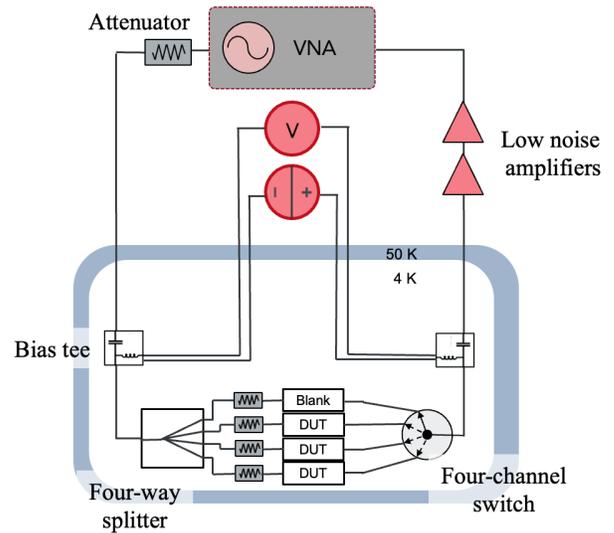


Figure 4. Experimental setup used to perform DC and RF characterisation of the test devices.

IV. RESULTS AND DISCUSSION

Fig.5 shows the results obtained from a 100-junctions chip with a junction area $A_{JJ} = 0.5 \mu\text{m}^2$ and a critical current density $J_c = 3.4 \text{ kA/cm}^2$. As shown in Fig.5(a), we managed to measure a clean RF transmission spectrum up to 10 GHz. We believe the deterioration of the transmission at higher frequencies is related with the way we mount our chip on the PCB, which is not optimal at the moment, as it requires long and bended bond-wires. Note that the observed feature around 7 GHz are artificial, originated from the calibration data using the blank sample. The unexpected dip at 3 GHz is under investigation at the moment, but should not affect our conclusion in this paper.

When we applied a DC current through the device, the RF spectrum barely changes until we reach $I_{DC} = 140 \mu\text{A}$, where the transmission starts to drop, reaching values lower than -15 dB for $I_{DC} = 160 \mu\text{A}$. This behaviour is consistent with the result obtained from the DC characterisation of the device, plotted in Fig.5(b) where the device exhibits no resistance until $I_{DC} \sim 140\text{-}160 \mu\text{A}$. Furthermore, when a single 3 GHz frequency tone ($P_{in} > -25 \text{ dBm}$ at the device's input port) is applied, we observe a 3rd harmonic generation without unwanted 2nd harmonic tone, suggesting that the transmission

line exhibits the expected Kerr-3 (χ^3) non-linearity required for 4-wave mixing.

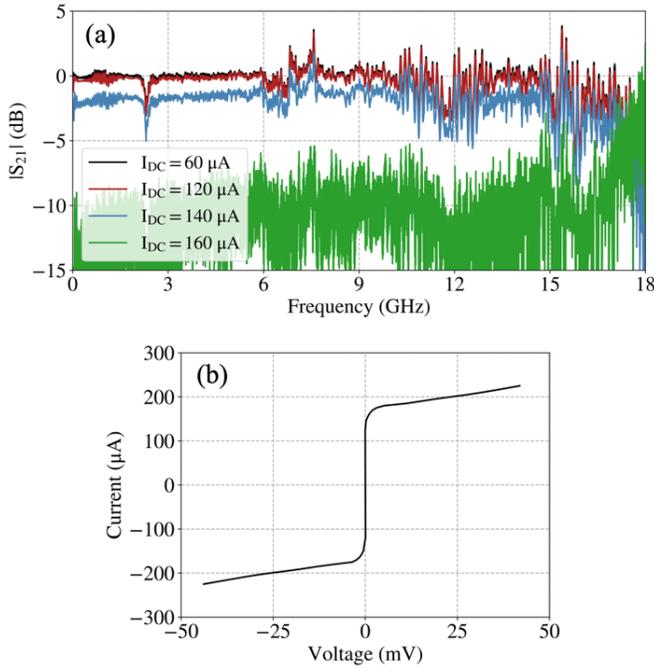


Figure 5. Characteristic for the 100-junctions device with $A_{JJ} = 0.5 \mu\text{m}^2$ and $J_c = 3.4 \text{ kA/cm}^2$ measured at 4 K. We set the VNA signal power to $P_{in} = -20$ dBm with a 30 dB attenuator installed in the input line. (a) The S_{21} transmission profiles of the device under DC current biasing conditions. (b) Measured IV curve of the chip.

The DC and RF measured results for a 500-junctions sample with $A_{JJ} = 0.5 \mu\text{m}^2$ and $J_c = 2.5 \text{ kA/cm}^2$ is plotted in Fig.6. The transmission measurements reveal a ripple effect as expected from the impedance mismatch generated by the CPW section loaded with junctions without additional features, which has a characteristic impedance higher than 50Ω . The DC IV-curve characterisation plotted in Fig.6(b) shows a gap voltage V_g of about 500 times higher than the V_g of a single Nb-AlO_x-Nb junction, i.e., $V_g = 2.8 \text{ mV}$; again, as expected. Fig.6(b) also shows an I_c value of $10 \mu\text{A}$, very close to the expected value of $I_c = 12 \mu\text{A}$ for the junctions with $A_{JJ} = 0.5 \mu\text{m}^2$ from this set of devices.

Given the encouraging results presented in Fig.6, we further tested this chip to search for possible gain, albeit with an expectation of a very small gain due to the short length of the device. Since the number of junctions is small and the critical current is higher than designated, we first estimate the expected gain for this device using the couple mode equations (CME) [8], assuming a shunt capacitance of $C_s = 1 \text{ fF}$ obtained from simulations of similar devices in Sonnet [9]. The results plotted in Fig.7(a) suggest that under this condition we should observe a gain up to 0.5 dB when pumping our device at 12 GHz, provided that the pump is very close to the I_c limit of the device. Similarly, a smaller gain below 0.1 dB should be observed when pumping the device at 6 GHz.

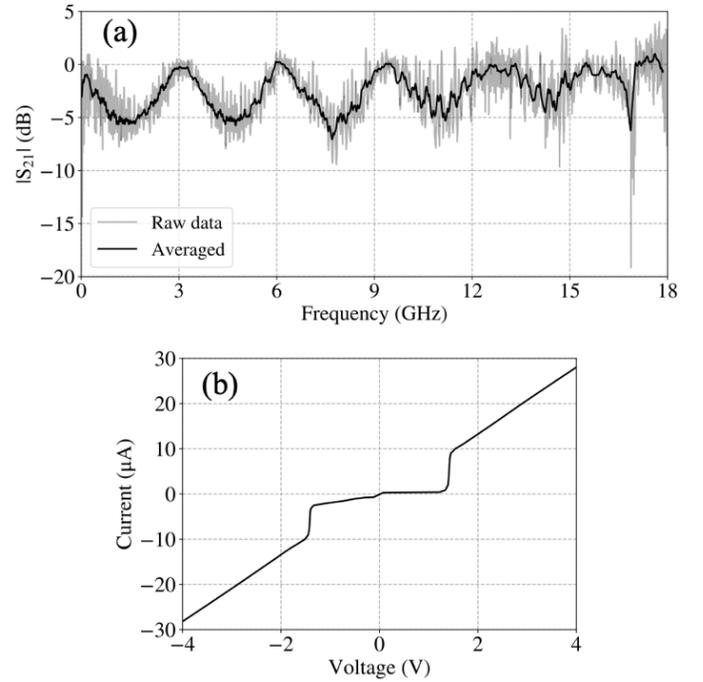


Figure 6. Measured results for a 500-junctions device with $A_{JJ} = 0.5 \mu\text{m}^2$ and $J_c = 2.5 \text{ kA/cm}^2$ at 4 K. We set the VNA signal power to $P_{in} = -20$ dBm with a 30 dB attenuator in the input line. (a) RF transmission of the device. (b) Measured IV curve of the chip.

We performed the gain measurement of the device, where we input two signals using a power combiner at room temperature. One port of the power combiner is swept using a VNA with 50 dB attenuation, while the other port of the combiner is connected to a signal generator providing the pump tone. The output of the device under test is amplified using two low-noise amplifiers at room temperature and fed to the second port of the VNA for characterisation. Fig.7(b) shows the gain values measured when pumping the device at 6 and 12 GHz with $P_{in} = -45$ dBm and setting the power of the sweeping signal of the VNA to -20 dBm, i.e., -70 dBm at the power divider's port. Although the gain results are very noisy, given the extremely low power signal required to maximize the ratio between the pump amplitude and the signal for an optimal gain, we did indeed observe gain consistent with our theoretical expectation. Note that our theoretical calculations do not consider the impedance mismatch of the line, hence the lack of rippling effect shown in the simulated result. But the measured gain profile does indeed show a similar ripple periodicity as observed in the unpumped transmission profile of the chip, indicating that the gain is most probably real. More importantly, the peak gain is close to the value we expected from the simulation. The slightly lower gain values measured compared to our calculations is most probably caused by the pump depletion and additional losses of the line.

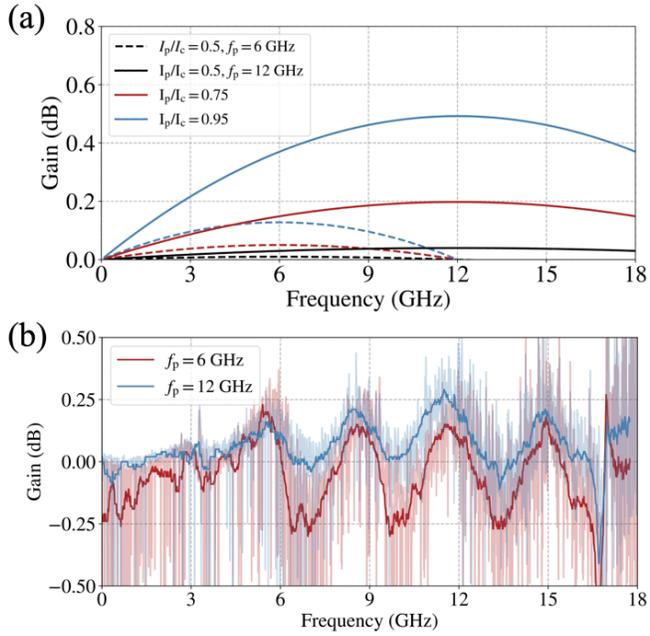


Figure 7. (a) Gain calculated using the analytical expression of the Couple Mode Equations (CME) for a 500-junctions device with $A_{J1} = 0.5 \mu\text{m}^2$ and $J_c = 2.5 \text{ kA/cm}^2$ when pumped with a pump at 6 GHz (dotted line) and 12 GHz (plain line). The different colours represent different amplitudes of the pump tone. (b) Measured gain for a 500-junctions device with $A_{J1} = 0.5 \mu\text{m}^2$ and $J_c = 2.5 \text{ kA/cm}^2$ when pumped with a strong tone at 6 GHz (red line) and 12 GHz (blue line). The raw data is plotted using light colours, while the darker lines correspond to a moving average of the data. We define the gain as the ratio of the transmission when the pump tone is on and off.

V. CONCLUSION

In this paper, we investigated the feasibility of utilising the tri-layer SIS junction fabrication technique for JTWPAs using a set of test devices. From the preliminary DC and RF characterisations, we observed a satisfactory transmission at frequencies below 10 GHz. We measured the DC and RF characteristics for a 500-junctions device, where the gap voltage shown to be 500 times the gap voltage of a single Nb-AlO_x-Nb junction as expected, and the critical current coincides with the value predicted. Finally, this device showed a measured gain consistent with theoretical calculations, demonstrating the potential use of the tri-layer tunnel junction technology for the fabrication of JTWPAs.

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