Design and Simulation of a Ultra-Wideband 211-375 GHz SIS Mixer based on a Micromachined Metallic Substrate

C. López, V. Desmaris, D. Meledin, A. Pavolotsky and V. Belitsky

Abstract—**In this paper, we describe the design and simulation of a novel ultra-wideband SIS mixer for radio astronomy applications, specifically to cover the ALMA telescope's bands 6 and 7 corresponding to an extensive 56% fractional bandwidth. The design features an electroplated metallic substrate that integrates a finline waveguide-to-substrate transition. Furthermore, the design employs a twin-junction SIS configuration with an Al/AlN barrier. The simulation of the RF matching circuit predicted a 93% coupling efficiency across most of the band. Additionally, this paper details the development and simulation of an integrated IF output circuit, optimized for the 4-16 GHz band. The simulation of the IF output circuit shows the losses in the IF coupling are better than 0.3 dB for most of the band and a reflection coefficient for a 50 Ω output impedance of -15 dB.**

Keywords—**SIS mixer, Broadband, Finline, Simulation.**

I. Introduction

IN the ever-evolving field of mm and sub-mm radio astronomy instrumentation, the technological development of wideband low-noise receivers has been the main focus of research over the last decades. Specifically, the ambitious goals set for the Atacama Large Millimeter/submillimeter Array (ALMA) in the 2030 roadmap [1], striving for a threefold improvement of the IF band, imply a de-facto need for receivers that can cover multiple frequency bands simultaneously, such as bands 6 (211–275 GHz) and 7 (275–373 GHz), i.e., a total a 55.5% fractional bandwidth. The mixers employed at these frequencies rely on superconductor-insulator-superconductor (SIS) technology due to its outstanding sensitivity at millimeter and sub-millimeter-waves [2][3]. Historically, designing SIS mixers, local oscillator sources (LO), and RF components [4-9] with a fractional bandwidth greater than 44% has been challenging. Although various examples in the literature demonstrate SIS mixers exceeding 40% fractional bandwidth [10-13], only a few have surpassed 55% fractional bandwidth, e.g. [14]. The majority of such mixers are based on traditional designs that employ an E-probe waveguide-to-substrate transition [3]. While these designs remain effective for smaller fractional bandwidths, they face limitations for larger bandwidths. Specifically, they require precise machining of waveguide backshorts, reduced height waveguides that increase RF losses [14], or the addition of waveguide capacitive elements in the input waveguide to increase the bandwidth [13]. Additionally, the tolerance for mounting the mixer chips and thus E-probe is a critical parameter for optimal mixer performance.

This paper addresses the design of a wideband SIS mixer in the 211-375 GHz range, i.e., targeting a 56% fractional bandwidth. Our mixer design does not employ a conventional dielectric substrate; instead, the Nb-Al/AlN-Nb SIS junctions [15] and RF matching circuitry are supported by an electroplated metallic substrate. This approach offers multiple advantages over dielectric substrates, e.g., avoiding the excitation of unwanted substrate modes, reducing dielectric losses, and naturally achieving chip grounding, while allowing substrate shaping. The latter facilitates the integration of a metallic finline seamlessly with the substrate. Furthermore, the absence of a dielectric substrate between the fins eases the matching over a wide bandwidth [4]. In addition, finline structures do not use waveguide shorts and demonstrate greater tolerance for the precision of mounting with respect to positioning in the waveguide, simplifying block fabrication requirements. Moreover, our design partially integrates the Intermediate Frequency (IF) output circuit for the 4-16 GHz band, including an extraction pad shaped as a landing capacitor that functions as an IF circuitry tuning component. This integration eliminates the need for additional lumped capacitors, simplifying the IF extraction process.

II. Mixer Chip Overview

The proposed broadband SIS mixer utilizes a metallic finline waveguide-to-substrate transition [4], seamlessly integrated into the substrate. The finline structure is positioned on the split-block plane of a 760 µm x 380 µm rectangular waveguide, as depicted in Fig. 1a. The metallic finline [16], matches the high impedance of the rectangular waveguide to a 100-ohm slotline. However, this impedance is still too high to properly

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match the SIS's low RF impedance, which is close to 11 ohms at the center frequency of 293.5 GHz. Therefore, further impedance transformation is necessary. Fig. 1b illustrates the employed transmission lines in the RF matching network. Slotlines 1 and 2 reduce the impedance from 100 Ohm to 60 Ohm, better suited for a slotline to microstrip transition. The silicon layer, with its high dielectric constant ($\varepsilon r \sim 11.3$) [17], is retained in this chip area to help lower the slotline impedance, thus facilitating the transition to a microstrip. The slotline-microstrip transition uses a 3rd-order Marchand Balun [5], formed by slotlines (3) and (4) and microstrips (5) and (6), as shown in Fig. 1b. Additionally, microstrips (6) and (7) create a 2-step Chebyshev transformer that completes the RF impedance transformation, enabling a broadband impedance match to the SIS junctions where the mixing process occurs. The mixer design, shown in Fig. 1a, employs twin SIS junctions to significantly ease the matching of the RF imaginary part impedance. The IF circuit, integrated into the same chip, is displayed in Figure 1b. The IF signal is extracted from the Marchand Balun transition using an RF filter that presents a high impedance to the RF signal, utilizing suspended microstrip lines over substrate cavities. The IF bandwidth is designed to be 4-16 GHz.

The mixer's various layers are detailed in Fig. 1c. As previously stated, the dielectric substrate is not entirely removed but remains in two areas of the chip: over the slotline-to-microstrip transition and at the suspended microstrip lines of the IF output. The 30 µm thick silicon layer is preserved to assist in impedance matching, provide structural support for the suspended microstrip, and enhance design robustness. Additionally, the chip incorporates two SiO_2 areas with different thicknesses. The first area, 250 nm thick and depicted in green, serves as a dielectric layer for the microstrip inverter of the SIS twin junction [18] configuration and a single section of impedance transformation. The second SiO_2 area, depicted in red and 650 nm thick, is used in both the Marchand balun and RF filter areas. This thicker SiO_2 layer reduces the overall capacitance seen by the IF system, thereby achieving a wider IF band. The electroplated metallic finline, made of 30 µm thick electroplated metal covered by 300 nm of Nb, acts as a counter electrode for the microstrip line. The finline chip's total length is 2420 µm, as shown in Fig. 1c.

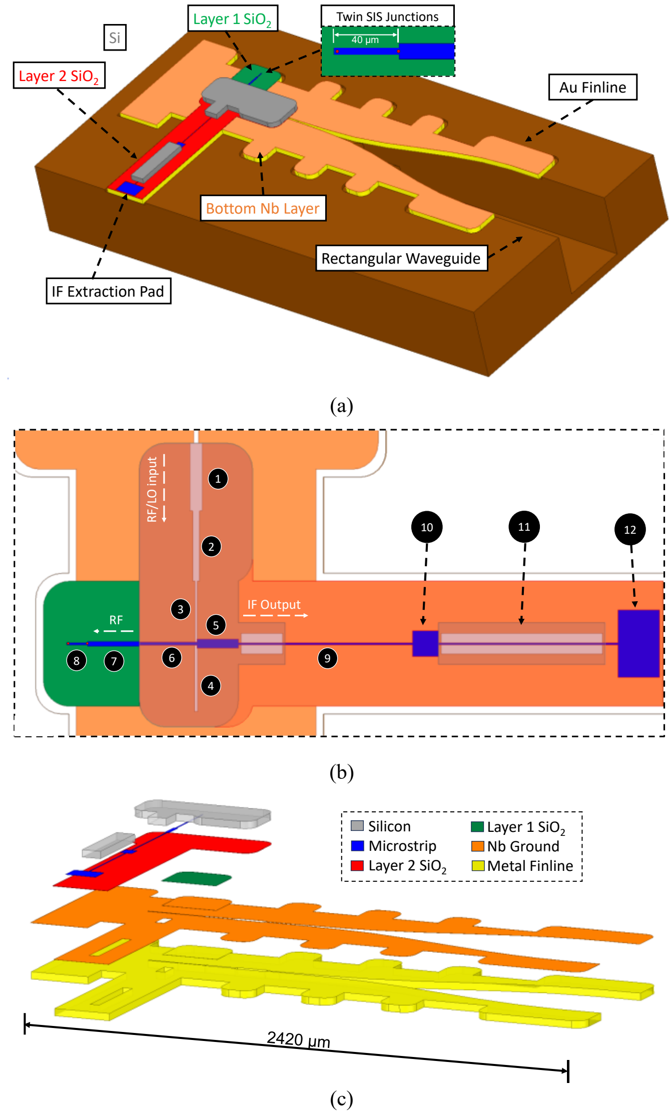

Fig. 1. Proposed broadband finline Mixer. (a) Mixer chip mounted in the split block. The rectangular waveguide is 760 µm x 380 µm. Detail of the different materials employed for the mixer chip fabrication. The twin junction configuration consist on 2 SIS junctions separated by a section of microstrip of 40 µm long and 4 µm width that serves as impedance inverter. (b) Top view of the slotline to microstrip transition and the integrated IF circuitry. For clarity the Si layer and the second SiO_2 layer are transparent. (c) Exploted view of the mixer chip that detail the layer layout and the different materials. The overall chip length is 2420 um.

III. RF Design

The proposed design utilizes a twin SIS junctions configuration [18] with a targeted RnA product of 14 Ohm·µm² and a nominal area of 1 µm². The twin junction configuration offers a broader bandwidth compared to a single junction, as the imaginary impedance of each junction can be offset by an impedance inverter. In our design, this inverter is comprised of a microstrip measuring 40 µm in length and 4 µm in width, placed over a 250 nm layer of SiO2. Additionally, the design incorporates SIS technology with an AlN tunnel barrier, offering lower capacitance at a given current density than Al-AlO_x tunnel barrier junctions [19], crucial for a wide IF response. The specific junction capacitance, calculated from

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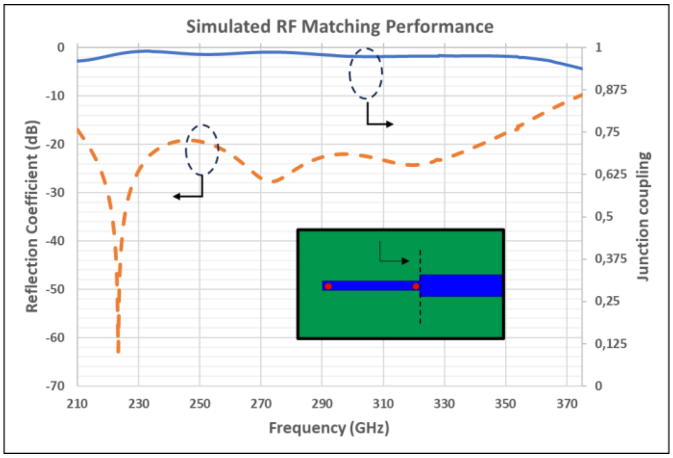
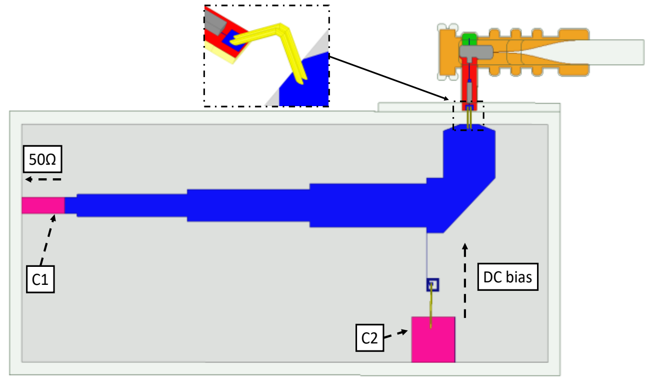


Fig. 2. Simulated performance of the RF matching circuit. For the HFSS simulation a lumped port was located as illustrated by the miniature. The impedance values for the twin junction circuit where calculated and load in the lumped port.

[20], is Cs=64.4 fF/µm². For the chosen area of 1 µm², the total capacitance from the twin junction amounts to 128.8 fF/µm². With the knowledge of Rn and the SIS capacitances, the RF admittance of the SIS junction is calculated using the quantum theory of mixing as outlined in [21]. According to this theory, all higher harmonics of the local oscillator signal are short-circuited by the junction capacitance, leading to the predominance of junction capacitance over the RF susceptance of the SIS. Consequently, the calculation of the quantum conductance provides a comprehensive understanding of the SIS RF impedance for a DSB mixer operation. At the central frequency of the mixer, i.e., 293.5 GHz, the RF resistance for a single SIS is approximately 11.6 Ohm, reducing to half if there's perfect cancellation of the imaginary part. Using a single-section transformer to match this low impedance to the 45 Ohms output of the Marchand balun is insufficient for a broadband performance. Therefore, a 2-section Chebyshev transformer, consisting of lines (6) and (7) as shown in Fig. 1b, was utilized. However, this approach has the drawback of increasing the capacitance seen at IF, effectively limiting the maximum IF bandwidth. To mitigate this issue, the first stage of the transformer is implemented with a thicker 650 nm layer of SiO_2, effectively lowering the total capacitance for the IF circuit. It's important to note that the differences in SiO_2 thickness do not create a vertical step in the superconducting Nb microstrip, as such a step could lead to electromagnetic discontinuities and potentially introduce an unwanted superconducting weak link affecting overall performance. This issue is circumvented as the device is fabricated starting from the silicon layer and concluding with the electroplating of the metallic finline.



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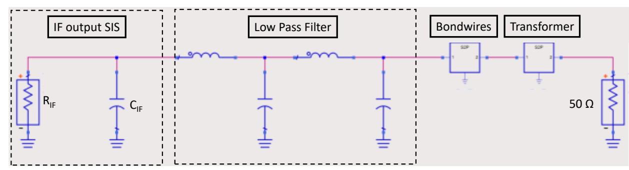
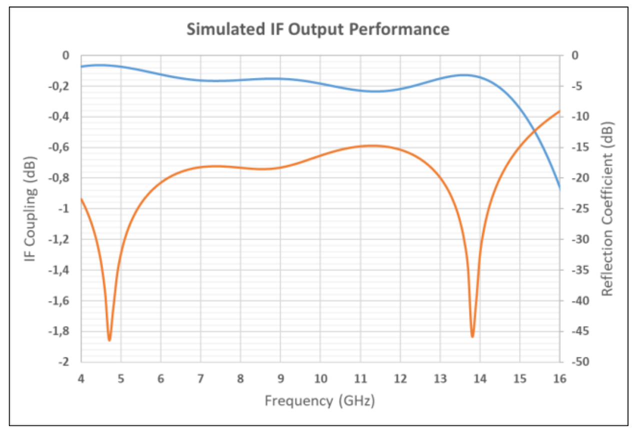


(b)



(c)

Fig. 3. IF output . (a) IF layout. The IF signal is extracted from the mixer chip with the help a 2 paralel bondwires. A 20 Ω to 50Ω impedance tranformer with integrated Bias T is employed. (b) Schematic of the IF circuitry. (c) Simulated performance for the IF Output circuit. to avoid cluttering.

The simulation of the mixer was conducted in the full wave 3D simulator Ansys HFSS (high-frequency structure simulator) in two phases. Initially, the RF impedance for a single SIS was calculated, followed by a simulation to determine the optimal length and width for the twin-section inverter. Upon identifying these parameters, the input complex impedance of the twin junction for the RF band 211-375 GHz was calculated. These values were then integrated into HFSS using a lumped port at microstrip (7), as depicted in Fig. 2. The model was

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subsequently fine-tuned to maximize both the coupling to the twin junction and the bandwidth. Fig. 2 demonstrates that the coupling level to the twin junction circuit exceeds 93%, indicating a reflection coefficient better than -15 dB for most of the targeted bandwidth.

IV. IF Output Circuit Design

The IF output circuit is partially integrated into the mixer chip and was designed to cover the 4-16 GHz band. In Fig. 1b, lines 9 to 12 form an RF/LO filter. Additionally, the IF circuit employs a 20 Ω to 50 Ω transformer, as illustrated in Fig 2.

To calculate the IF response, both the IF impedance of the mixer chip (parallel combination of real and imaginary parts, R_{IF} and C_{IF}, respectively) needs to be known. The IF output impedance of an SIS junction is determined by the slope of the pumped IV curve [21], typically 8-10 times the Rn values. To prevent excessive conversion gain and ensure stable operation of the mixer, the IF load impedance was set 20 Ω, using a transformer from 50 Ω. Meanwhile, C_{IF} was calculated from the junction capacitances and the geometric capacitance of the RF tuning circuitry, resulting in a total capacitance of 376 fF.

The twin junction configuration lacks a natural "cold point" for extracting IF signals. This issue can be addressed by using an LC circuitry realized as a high-impedance line with a landing capacitor in conjunction with bondwires [22]. In our mixer design, the IF signal extraction uses a mix of high and low-impedance lines to form a low-pass filter that effectively rejects the RF/LO signal. The first section of this filter is marked as 9 in Fig. 1b. The electroplated metal's flexibility allows for the creation of small cavities in the substrate to form suspended microstrip lines with high impedance to the RF/LO signal. The filter is completed by a low-impedance line (10), a second section of suspended microstrip line (11), and the IF contact/ extraction pad (12). It's important to note that the filter is situated on top of the 650 nm SiO2 area to minimize the added capacitance to the IF output. The structure acts as an LC filter for the IF signal, as shown in Fig. 2b. The output performance is influenced by the inductance of the bondwires used in the IF extraction circuitry, necessitating a detailed 3D simulation including the bondwires for accurate performance prediction. Two parallel bondwires, as seen in Fig. 2a, were used to decrease the inductance added to the output LC filter.

The IF extraction is completed with a multisection superconducting transformer on a 254 μm thick alumina substrate. This transformer, shown in Fig. 2a, incorporates a bias T consisting of a DC blocking capacitor (C1) and an IF shunting capacitor (C2). The latter works in tandem with a spiral inductor and a high-impedance line as a stop filter for the IF signal.

The simulated performance of the complete IF output circuit is shown in Fig. 2c. The graph indicates that the losses in the IF coupling is below 0.3 dB for most of the band, and the reflection coefficient is below -15 dB for the majority of the IF band.

V. Conclusion

In this paper, we present a novel broadband SIS mixer design targeting the frequency range of the ALMA telescope's current bands 6 and 7, i.e., 211-375 GHz. While existing SIS mixer designs employing traditional transitions and substrates have achieved significant fractional bandwidths, the research into alternative wideband solutions remains a critical topic for the future of radio astronomy receivers. The design presented in this paper not only addresses current limitations but also opens new opportunities for the development of prospective SIS mixer technology. The presented mixer chip represents a significant shift from traditional design approaches by eliminating the use of a dielectric substrate and replacing it with an electroplated metallic substrate, facilitating the integration of a metallic finline. The suggested design and simulations of RF matching circuits for a twin junction SIS configuration, achieve a simulated coupling of over 93% for most of the frequency band. Additionally, we detail the design of the IF output circuit, which is directly integrated onto the mixer chip. The IF performance, simulated for the 4-16 GHz band, shows a coupling loss better than 0.3 dB for most of the IF bandwidth.

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