Improved Process Flow of Heterogeneously Integrated Gallium Arsenide Schottky Diodes

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***Abstract*— An improved process flow for fabricating heterogeneously integrated gallium arsenide Schottky diodes on membranes of 15 µm thick high-resistivity silicon microstrip substrate is reported. This effort has three focuses: 1) optimizing the fabrication of devices with high packing density to maximize devices per run, 2) co-fabrication of beam leads and side wall-Au plated vias, and 3) simplifying the process by reducing the number of processing steps.**

***Keywords*—GaAs Schottky Diode fabrication, microstrip, vias, beam leads, Silicon on Insulator, SOI**

I. INTRODUCTION

High-frequency radars, spectrometers, and radiometers employ frequency multiplication chains for local oscillators pumping mixers to receive high-frequency signals [1]. These multiplication chains usually comprise a cascade of doublers, triplers, [2]and mixers implemented in separate waveguide blocks. This modular packaging leads to larger system sizes. The heterogeneous integration of devices onto silicon can significantly miniaturize these systems by implementing cascaded multipliers and mixers on a common substrate, resulting in compact sub-mm wave electronics. The main goal for the resulting chips is to improve thermal dissipation, efficiency, and power output, resulting in smaller, more efficient systems with more output power.

Progress has been reported on the heterogeneous integration of these components onto a common chip; however, the complicated fabrication process limited yields. A new process has been developed utilizing a microstrip substrate with side wall-Au plated vias co-fabricated with beam leads. This new process results in better yields, thermal management, and power handling that may eliminate the need for additional power amplification and cooling systems, making it of particular interest to the space industry and manufacturers of consumer-grade electronics.

The diodes presented in this work were fabricated on a 15 µm thick high resistivity silicon microstrip substrates, with side wall-Au plated vias, and beam leads. This preliminary work is to verify that this process flow can be standardized and used to create highly integrated components on a single chip. This paper reports an enhanced process flow adapted from Nadri's and Xie's work in integrating GaAs Schottky diodes onto thin silicon [3], [4].

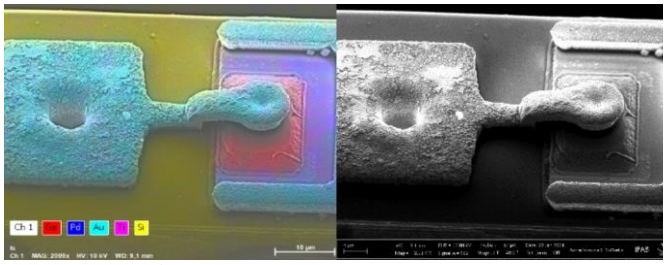

Fig. 1. Shown left is an Electron Dispersive Spectroscopy measurement highlighting the different material sections of the diode structure, asernide is hidden to provide contrast. Shown right is a Scanning Electron Microscopy measurement of the same diode. Both have the same structure, which shows the side wall-Au plated vias and the Schottky Diode.

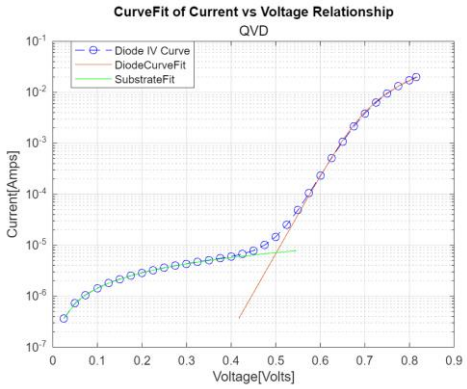

Fig. 2. The diode current-voltage relationship shows approximately Rs=4.6, Ideality=1.13, and Isat=1.4e-13. The ideal series resistance is 1.54 ohms. Measurement was taken with a 2pt probe. Curve fitting was done in Matlab via a nonlinear least square fitting. R-square=0.998 Root Mean Squared Error=.0045

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II. FABRICATION

The fabrication process employed to create these chips involves a unique epitaxy transfer method for bonding GaAs material to a silicon-on-insulator (SOI) substrate to create Schottky diodes [4]. A GaAs epitaxy on a semi-insulating 650 µm GaAs handle featuring an AlGaAs etch stop layer, n-GaAs, n+-GaAs device layers, and a 90 nm highly-doped ($>10^{19}$ cm^{-3}) graded $In_xGa_{1-x}As$ cap layer (x:0→0.6) was used for the diode.The procedure used to create the devices is adapted from the process described in reference [5]. The process is started by first depositing a titanium, palladium, gold, and titanium (Ti/Pd/Au/Ti) (20/40/150/20 nm) ohmic metal layer onto a GaAs wafer with electron beam physical vapor deposition. The 15 µm thick high resistivity SOI wafer is then bonded onto the ohmic metal layer using SU-8. The GaAs handle removal is a 4-step process: Argon ion mill, followed by a nitric-based etch, a citric-based etch step, and a hydrofluoric acid-based etch for the AlGaAs etch stop layer. Photolithography and a citric based etch form the GaAs mesas. The ohmic pedestal was formed using a combination of dry and wet etches. A CF_4/Ar RIE etch, optimized for high selectivity to photoresist, Pd, and Si, was engineered for etching Ti and SU-8. Transene Gold Etch Type A is used to etch Pd and Au. The optimized etch processes developed in this work results in a high resistivity silicon surface with only ohmic pedestals and GaAs Mesas, without etch residue and minimal etching of the silicon substrate.

Lithography and a Bosch etch were used to form 11 µm diameter vias. A sacrificial resist is spun and exposed to define the geometry for the Schottky diodes. A thin layer of Ti (~15 nm) and Au (~30 nm) was deposited by magnetron sputtering to form the diode contact. Then, lithography defines the topside metallization, beam lead, and airbridge features. O_2 plasma cleans the developed features before electroplating. Electroplating coats a 3.5 µm thick Au layer using Technic gold solution. Ultrasonic agitation and a magnetic stir bar ensure a smooth surface finish and side wall metallization of defined vias. A combination of WaferBOND and epoxy was used to create a semi-permanent bond of the wafer to a Si carrier, allowing debonding and release of the final chips. The silicon handle was removed through lapping, plasma etching, and a buffered oxide etch (BOE). The microstrip ground plane is formed on the high-resistivity silicon's exposed backside in a photolithography and electroplating step. Photolithographic and DRIE processes are used to define the chip's outlines, allowing the precise formation of complex chip geometries not possible through traditional dicing techniques [6]. The finished chips are released through a heated solvent-based debonding process. Figure 1 shows an SEM image of the fabricated diode structure. The measured and curve-fitted current and voltage relationship of the diode is shown in Figure 2. Figure 3 shows the design drawing for comparison.

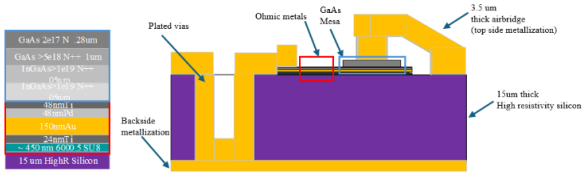

Fig. 3. Side profile of quasi-vertical fabricated for this work

III. CONCLUSION

This paper reports an enhanced and novel process flow optimizing the fabrication of quasi-vertical Schottky diodes on a thin microstrip substrate. In comparison to previously reported processes, this eliminates the need for multiple GaAs etches, reduces the amount of etches required for the ohmic metal stack, selectively etches the ohmic layers without significantly etching the resist and silicon, and significantly reduces residual etch byproducts of fluorine-based etches. This work also reports a heterogeneously integrated Schottky diode fabricated on a thin microstrip incorporating 11 µm side wall-Au plated vias alongside suspended beam leads, accomplished by sputtering and electroplating.

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