# A Planar RF-LO Coupler Design for Heterodyne Receiver at 220 GHz

Yan-Jun, Wang[1,2], Chun-Lun Wang[2], Chao-Ching Wang[2], Yu-Chieh Huang[2] and Ming-Jye, Wang[2*]

[1] *National Taiwan University, Taipei, 10617, Taiwan;*

[2] *Institute of Astronomy and Astrophysics, Academia Sinica, Taipei 10617, Taiwan*

[*]*Corresponding author: Ming-Jye Wang, mingjye@asiaa.sincia.edu.tw*

Abstract

A planar 220 GHz directional coupler, comprising two distinct layers of microstrip lines (MLs) with an overlapping section, has been designed. The length of this overlapped section allows for the adjustment of coupling efficiency between the two MLs. This planar directional coupler, intended for coupling radio frequency (RF) and local oscillator (LO) signals, can be integrated with mixers to create a compact heterodyne receiver. Such a receiver is highly desirable for constructing large-format multi-pixel array receivers at millimeter and sub-millimeter wavelengths. The detailed design of the 220 GHz directional coupler and its scaled model, operating at 10 GHz, are presented. Preliminary measurement results of the scaled model confirm the feasibility of this concept, although some external issues still need to be resolved.

*Keywords*—Heterodyne receiver, Directional coupler, Planar circuit

## Introduction

Integrating electrical components on a chip is a modern approach to building complex circuits with optimized space utilization. This concept can also be implemented in heterodyne receivers at sub-millimeter wavelengths. A heterodyne receiver typically requires many waveguide components, such as directional couplers, local oscillator power distributors, and orthogonal mode transducers. Optimized components are selected to assemble single-pixel receivers for the best performance. These high-performance single-pixel receivers are deployed on the elements of interferometers. However, there is a high demand for multi-pixel heterodyne receivers for large aperture telescopes. A few multi-pixel heterodyne receivers have been developed and deployed on telescopes, such as Nobeyama-BEARS (25 pixels), Delinha (9 pixels), JCMT-HARP (16 pixels), and SuperCAM (64 pixels), APEX-CHAMP+ (14 pixels), and IRAM-HERA (9 pixels). Some new multi-pixel receivers are currently under development. The architecture of these multi-pixel receivers is similar to that of single-pixel receivers, which makes scaling the pixel number up to 100 very challenging for 50-meter class telescope in the future.

Recently, Shan et al. demonstrated a two-pixel heterodyne receiver chip operating at 140-170 GHz using planarized circuits to replace most waveguide components [1]. This compact design makes constructing large-format multi-pixel receivers more feasible, although the receiver's performance is not yet optimal. However, in their design, the local oscillator (LO) power is injected into each mixer through waveguide coupling, requiring four waveguides for LO distribution. By designing a planar LO power distribution circuit that incorporates an LO/RF coupler for each mixer, the receiver would require only a single waveguide for LO power, making the receiver even more compact.

In this paper, we present the design of a planar 220 GHz RF/LO directional coupler with two overlapped microstrip lines (MLs), inspired by the work of Tan et al. [2], who reported a directional coupler design with an overlapped section of coplanar-waveguide (CPW) and ML. Our design features an ML with a Z-bent section overlapping another ML on the bottom. The coupling coefficient is controlled by the length of the overlap. As a proof of concept, a scaled model chip operating at 10 GHz was designed, fabricated, and tested. The details of this design and its performance will be presented and discussed.

## Results and Discussion

A. Design of 200 GHz coupler

The basic design concept involves overlapping two microstrip lines (MLs) for a certain length. The electromagnetic (EM) fields of the two MLs in the overlapped region will couple to each other, and the coupling efficiency (CE) can be tuned by adjusting the coupling length (CL). An exploded view of the device structure is shown in Fig. 1(a). The upper ML, which is 6 μm in width, is bent to align with the lower ML, which is 3 μm in width. These three metal layers, made of 0.3 μm niobium (Nb), are separated by two dielectric layers of 0.3 μm silicon dioxide (SiO2). The impedances of the two MLs are designed to be 16 ohms. Fig. 1(b) shows the top view of the directional coupler and the definition of ports.

Figure 2 depicts the simulated S-parameters of the designed directional coupler using HFSS with six different coupling lengths (CLs). The return losses are consistently below -15 dB. Specifically, S41 represents the coupling efficiency (CE) from the LO to the RF port, ranging between -35 dB and -15 dB for coupling lengths from 5 μm to 30 μm. This relationship is illustrated in the inset of Fig. 1 (b). In mixer applications, the coupling efficiency of a directional coupler for LO/RF coupling typically hovers around -17 dB. For the 200 GHz model, a coupling length close to 20 µm achieves this coupling efficiency.

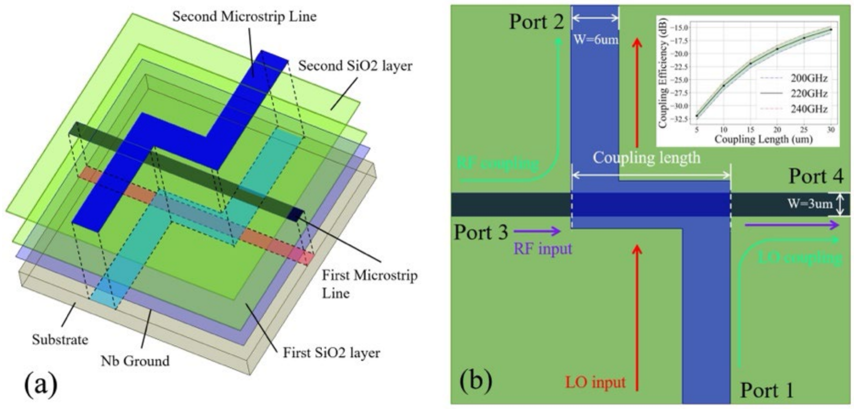


Figure 1 (a) Exploded view of the planar RF/LO coupler. (b) The top view of the planar RF/LO coupler and the definition of each port. The inset shows the relation between coupling efficient and coupler length.

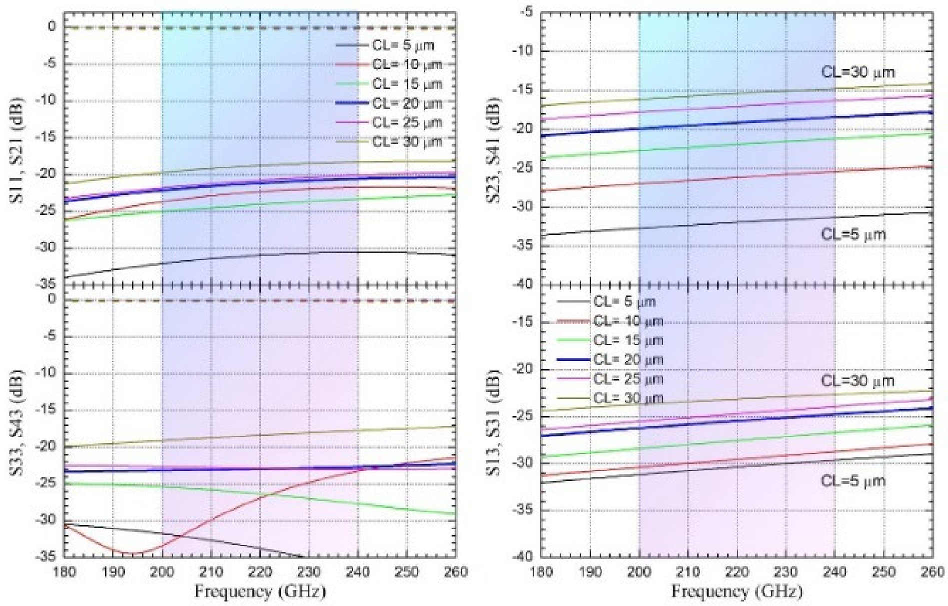


Figure 2 The simulated S-parameters of planar RF/LO coupler at 220 GHz central frequency. The operation frequency is set between 200 and 240 GHz (Blue area). S41 & S23 is the coupling efficiency

## B. Scaled Model

To verify the feasibility of our concept, a scaled model, adjusting the central frequency from 220 GHz to 10 GHz, was designed. The configuration of the coupler region (overlapped microstrip lines) is identical to that of the 220 GHz version, but the coupling lengths are scaled according to the wavelength. This scaled chip has been successfully designed and fabricated. In addition to the coupling region, matching circuits from MLs to coplanar waveguides (CPWs) and 50 Ω input/output ports were also designed, depicted on the left side of Figure 3. The comparison of coupling coefficients between the 220 GHz design (black line) and the scaled model (blue line) with varying lengths is shown in the middle of Figure 3. The simulated coupling efficiencies (CEs) of the 220 GHz coupler and its scaled models are displayed in Figure 1(b), revealing a CE difference of less than 1 dB between the two models. The scaled chip was mounted in a test block and connected to signal lines and ground using aluminum bonded wires, as illustrated on the right side of Figure 3.

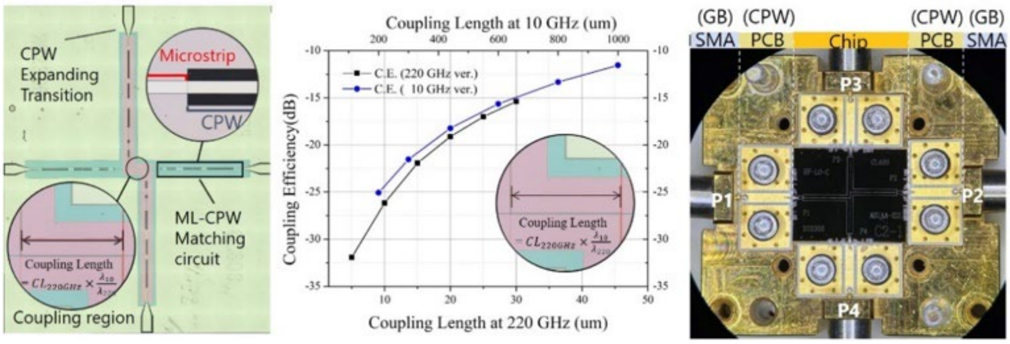


Figure 3 Left: The scaled chip with impedance matching circuits and input/output ports. Middle: The comparison of simulated coupling coefficient between the scaled model and 220 GHz chips. The coupling length was scaled by the wavelength. Right: The scaled chip mounted in the test block.

The performance of the scaled chip was evaluated in a cryostat operating at 2K, as depicted in the left side of Figure 4. The four ports of the scaled-model chip were connected to the feedthroughs on the chamber wall via 40.5 cm long coaxial cables. A vector network analyzer was employed to measure the directional coupler's performance. The simulated S-parameters are shown in blue lines, while the measured results are indicated by black lines in the right side of Figure 4. Generally, the LO and RF transmissions (S21, S43) exhibit values ranging from -1 to -3 dB across the 8-12 GHz frequency band. The LO and RF reflections (S11, S33) are notably worse than the anticipated values, suggesting an impedance mismatch within the system. The coupling (S23, S41) closely approximates the designed specifications, while the isolation (S13, S31) measures approximately 5 dB higher than simulated values.

In the raw data (black lines), two types of ripples, approximately 200 MHz and 3 GHz in frequency, suggest possible impedance mismatches within the circuit. To investigate this issue further, time-domain measurements were conducted for each port using a CL=600 μm chip. Figure 5 illustrates the results for Port 1 and Port 2 (upper panel) as well as Port 3 and Port 4 (lower panel). The impedance responses of Port 1 and Port 2 are nearly identical, and a similar consistency is observed between Port 3 and Port 4.

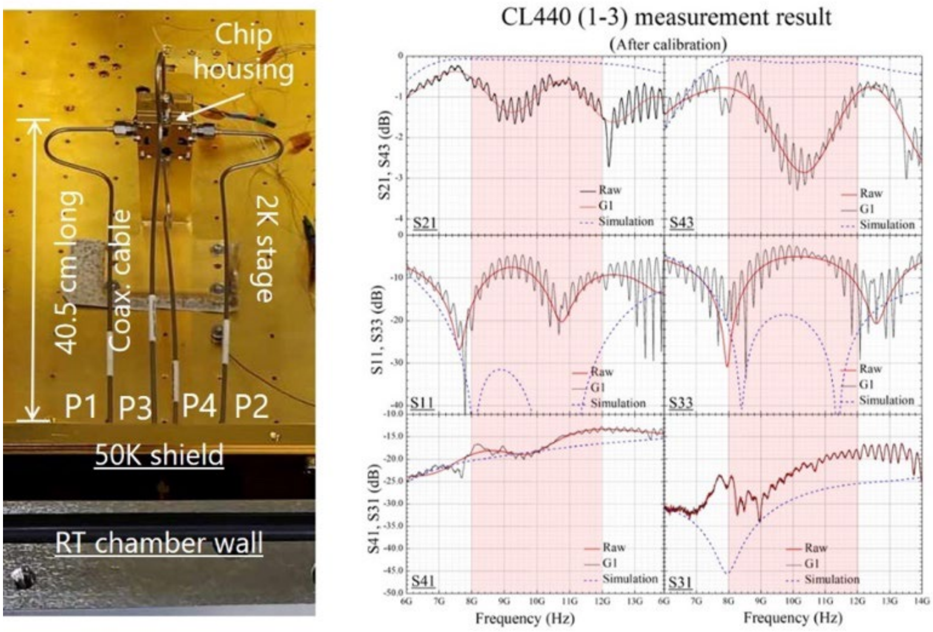


Figure 4 Left: The measurement setup of the scaled directional coupler. The chip housing was mounted on the cold plate (2 K) and it four ports were connected to the chamber wall by 40.5 cm long coaxial cables. Right: The comparison of simulated and measured S-parameters of scaled directional coupler with a coupling length of 440 μm.

To investigate the impedance mismatching issue further, time-domain measurements were conducted for each port. Figure 5 illustrates the results for Port 1 and Port 2 (upper panel) as well as Port 3 and Port 4 (lower panel). The impedance responses of Port 1 and Port 2 are nearly identical, as are those of Port 3 and Port 4. The longer transmission line in the design results in a longer time delay along Port 1(2) compared to Port 3(4). The responses in the coaxial connector (light red) and transition (light blue) regions are similar across all ports. The impedance of the metal layers for Port 1(2) and Port 3(4) measures approximately 21 Ω and 20 Ω, respectively, slightly higher than the intended design value of 16 Ω. A distinct step is evident in the chip region for Port 1(2), marked by a circle, but not observed for Port 3(4). Detailed time-gating measurements may shed light on the factors contributing to the poorer performance of S43.

After identifying impedance variations at different locations, the S-parameters were re-measured using time gating mode. The red lines on the right side of Figure 4 were obtained by gating between the connectors of two ports on the housing, denoted as “G1”. The ~200 MHz ripple noticeably disappeared upon gating, indicating it was likely caused by slight impedance mismatches between the housing and the four 40.5 cm long cables. However, gating at the location with the highest impedance did not eliminate the ~3 GHz ripple observed in S21 and S43.

The test results of the scaled chip successfully demonstrated our concept of using two overlapped metal layers (MLs) for the RF/LO directional coupler. The measured coupling strength closely matched the designed values. Fortunately, the absence of wire bonds in the 220 GHz chip may have mitigated impedance mismatch issues. Furthermore, it should be noted that the losses in the transmission lines were not accounted for in our initial simulations. These losses will be incorporated in future designs using a surface impedance model.

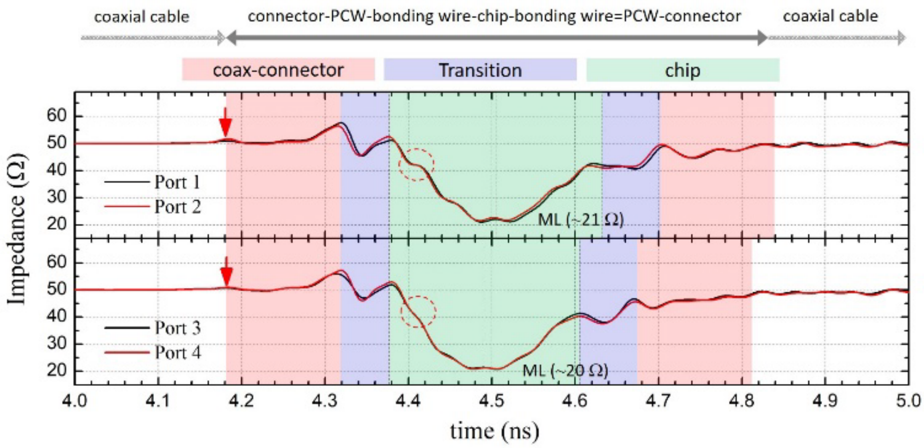


**Fig. 5.** The time domain measurement for Port 1&2 (upper panel) and Port 3&4 (lower panel). The red circle points out the main difference between two panels.

## Summary and Future Work

We presented a design for a planarized RF/LO coupler operating at 220 GHz, along with its scaled model. The coupling coefficient is adjustable through the overlapped length between two metal layers (MLs). Preliminary measurements indicate a reasonable performance of the scaled-model chip. However, the measured data was notably affected by multiple reflections due to impedance mismatches at the interfaces of the coaxial cables, housing, and bonding wires to the chip. The 220 GHz LO/RF coupler chip will be to fabricated and tested in the near future.

## Acknowledgement

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Reference


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