Embedding Impedance Recovery in a Twin- Junction SIS Mixer

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***Abstract*—We describe a method for calculating the embedding impedance of an SIS mixer employing twin junction tuning. Calculation of the embedding impedance is done using equivalent transmission line circuits of the mixer, the measured pumped and unpumped IV curves of the mixer chip and the Tucker theory expressions of the tunneling currents. Our simulation method does not require the individual IV curves of the two junctions.**

***Keywords*— Belitsky tuning, SIS mixer, Twin junction mixer.**

AN important step in the design of SIS mixers is the matching of the RF feeding circuit to the SIS junction which is made difficult as a result of the large capacitance of the junction. The mixer circuit therefore includes a mechanism for tuning out of the junction capacitance. An elegant design of this tuning mechanism is the twin-junction device which was proposed by Belitsky et al [1] and was subsequently employed in SIS mixers at several frequency bands. It consists of two parallel SIS tunnel junctions connected by a transmission line, typically a microstrip line. The principle of operation is based on the fact that when a transmission line with carefully selected length and characteristic impedance separating the two SIS junctions is used, the reactance of the two junctions can be made to cancel each other and the input impedance of the device becomes real, hence can easily be matched to the feeding RF circuit.

I. Method of Impedance Recovery

Recovery of the embedding impedance in SIS mixers is a powerful tool that allows assessment of the design of the mixer circuits, hence gives additional tools to improve the next version of the mixer chip design. Recovery of the embedding impedance of a single mixer has already been reported [2], [3] and several computational techniques were employed to implement the calculations, based on the knowledge of the device pumped and unpumped curves. Applying the same method for the twin- junction mixer is not straightforward since the transmission line connecting the two junctions causes them to be pumped at different levels and the currents flowing through the two junctions will have different phases. Nevertheless, we were able to express the twin junction arrangement in a simple Thevenin Circuit albeit the current through the device became more complex. The Thevenin equivalent circuit of a twin-junction mixer can be represented by the equation

$$V_{\mathrm{Source}} = V_{\mathrm{D}} + Z_{\mathrm{emb}} I_{\mathrm{D}} \,,$$

where V_{Source} is the voltage of the local oscillator, V_{D} is the complex voltage across the device and Z_{emb} is the embedding impedance. The current across the device can be written as

$$I_{\mathrm{D}} = I_1(V_0, |V_1|) + I_2(V_0, |V_2|)\cos(\beta l) + i\frac{V_2(V_0)\sin(\beta l)}{Z_0} \,,$$

where l, β and Z_0 are respectively the length, propagation constant and characteristics impedance of the microstrip line. The current I_k through each junction may be taken from Tucker theory but a phase multiple must be included:

$$I_k(V_0, V_k) = \sum_{n=-\infty}^{\infty} J_n(\alpha_k)[J_{n-1}(\alpha_k) + J_{n+1}(\alpha_k)] \left[I_{\mathrm{DC},k}(V_0 - nV_{\mathrm{Ph}}) + iI_{\mathrm{KK},k}(V_0 - nV_{\mathrm{Ph}}) \right] e^{i\phi_k} \,,$$

where V_0 is the bias voltage, V_k and α_k are respectively the magnitude of the voltage and the pump factor across either junction and ϕ_k is a phase factor. The other symbols have their usual meaning. Recovery of the embedding impedance can then proceed as described in the references but two transcendental equations are now needed to recover the two voltages across the two junctions. This can make calculation of the error surfaces lengthy but we developed software techniques that allows reasonably fast iterations.

We have demonstrated our method by recovering the embedding impedance of two twin junction SIS mixer, one operating at 230 GHz and the other at THz mixer frequencies. We compared the performance of several computational techniques and also discuss the influence of the IF circuit on the integrity of the computations.

References

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