Designs of Broadband Unilateral Finline SIS Mixers Employing 15 μm Silicon-On-Insulator Substrate at THz Frequencies

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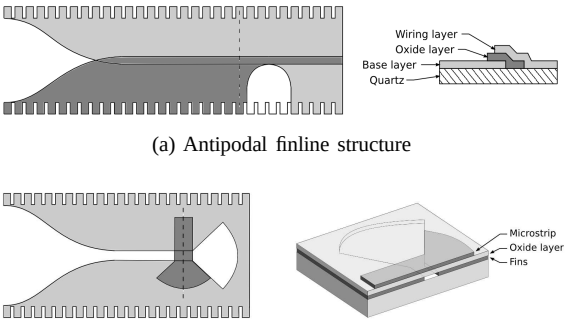
***Abstract*—We present the design of two niobium single-ended Superconductor-Insulator-Superconductor (SIS) mixers optimized to work in the frequency range of 600–700 GHz. A key feature of this new mixer design is the utilization of a unilateral finline taper. This transition is significantly easier to design and simulate than the previously employed antipodal finline, and more importantly it simplifies the chip fabrication considerably since the fins do not overlap at any stage. RF power propagating in the finline is coupled to the microstrip either directly from the slotline to microstrip, or more efficiently via a coplanar waveguide (CPW). Another novel feature of our design is the fabrication of the mixer chip on a very thin silicon substrate which will be achieved using Silicon-On-Insulator (SOI) technology. This will allow easy matching of the incoming signal from the feed horn to the loaded waveguide and allows the lightweight mixer chip to be held in the E-plane of the waveguide using gold beam leads, eliminating the need for a deep groove in the waveguide wall. These new features yield a significantly shorter chip and allow wider RF bandwidth since the excitation of higher order modes in the groove has been avoided. The mixer block is extremely simple, composing a smooth-walled horn and a waveguide section without any complicated mechanical features. In this paper, we present the details of the mixer chip, including various transition sections, tuning circuits and mixer block designs, supported by electromagnetic simulations. We describe the design procedure in detail and predict the full mixer performance using the SuperMix software package.**

I. Introduction

The next generation of astronomical instrument requires a mixer design that is suitable for large format imaging array architecture. The mixer should be easy to produce, repeatable, broadband and compatible with planar circuit technology. At submillimetre wavelengths, the finline-tapered mixer design which is compact and easy to fabricate offers a very attractive option to satisfy this requirement. Finline mixers do not require complicated waveguide structures and do not rely on mechanical tuners, i.e. backshorts or E-plane tuners. All the superconducting circuitry is fabricated using planar circuit technology. They have wide RF bandwidth and the large substrate area makes integrating additional mixer circuits elegant and simple.

One essential feature of the finline mixer is that the entire mixer, from the feed horn to the IF output of the mixer chip, lies along the same axis. The mixer chip is held along the E-plane of a split-block waveguide with a groove on the waveguide wall. The RF propagation path is oriented to the axial axis of the feed horn. This greatly simplify the design of a closed-packed imaging array, since the size of the whole mixer is completely defined by the footprint of the horn aperture. This becomes even more attractive at higher frequency.



(a) Antipodal finline structure

(b) Unilateral finline structure

Fig. 1. Finline diagram.

Traditionally, finline mixers use antipodal fins to couple RF signal from the waveguide to the microstrip line containing the miniature SIS tunnel junction. As shown in Figure 1(a), the metallisation for the base and the wiring layer is in the form of two niobium fins separated by 400 nm of oxide. The whole arrangement is deposited on a conventional 220 μm thick quartz substrate, which can occupy a substantial space in the waveguide. The resulting dielectric loading losses which increases with frequency makes this traditional finline mixers design less attractive at higher frequency band.

An antipodal finline mixer chip comprise of three distinct sections: the non-overlapping fins, the overlapping regions and the microstrip line. The first section tapers down smoothly the high impedance of an unloaded waveguide to match that of a superconducting microstrip line. This also transforms the RF from the waveguide mode into microstrip mode. When the fins starts to overlap, it behaves more like a parallel-plate waveguide with the effective width equal to the overlap region. The overlapping width is widened until it is large enough to ignore the fringing effects. This then slowly tapered to the required width of the microstrip line by a semicircular cutout, as shown in Figure 1(a). This technology had been fabricated and tested by Yassin et. al. [1], [2], [3] at various submillimeter bands.

They demonstrated state-of-the-art performance, comparable to the more conventional probe-coupled waveguide mixer.

Despite the excellent performance of an antipodal finline mixer, there are some shortcomings. The need of overlapping region makes the mixer chip longer, and is susceptible to shorting during the fabrication process. The electromagnetic behaviour of the mixer is also very difficult to simulate, making it hard to design. To overcome these difficulties, we have developed a new waveguide-to-planar circuit transition that replace the antipodal fins with a unilateral finline taper. Unilateral finline mixer retain all the above-mentioned advantages of an antipodal finline mixers, but have no overlapping taper region. This yield a shorter mixer chip, and hence reduce the losses and enable more devices to be fabricated on the same wafer. This will significantly reduce the time needed to produce a large number of mixer chips for a focal plane array.

As seen from Figure 1(b), the unilateral fins transform the RF power from the waveguide mode into a slotline without any additional complicated strutures. The narrow slotline on the other hand provides a natural band-pass filter to prevent the IF signal entering the mixer chip. The transition from slotline to microstrip or coplanar waveguide (CPW) can be done easily and are broadband as well. This design is straightforward and its electromagnetic behaviour can be easily simulated using conventional software package like HFSS or well-understood algorithms such as the Optimum Taper Method or Spectral domain analysis [4]. This has already been demonstrated in conjunction with Transition-Edge Sensors (TES) for CLOVER project [5] (fabricated at University of Cambridge [6]) and dhown to works very well.

Another novelty of our new mixer design is that the entire superconducting circuit is deposited on a 15 μm thick silicon substrate using the Silicon-On-Insulator (SOI) technology, which was not available until recently. This allows the thin mixer chip to be positioned across the split-block waveguide without a supporting groove in the waveguide wall, avoiding the excitation of higher order modes. The chip is simply supported by gold beam leads deposited on the substrate. Thin substrate decreases the dielectric loading losses, and allows the finline mixer design to be extended well into the THz regime. SOI technology also allows the mixer chip to be shaped into any desirable form using photolithography rather than dicing. This leaves more freedom in designing the matching notches, which are used to match the impedance of the air-filled waveguide to the loaded waveguide for broadband performance.

In this paper, we lay out the design of our unilateral finline mixer in Section II, and proceed to discuss in detail each component building up to the final mixer design. We emphasize the RF design procedure of the various transitions, the tuning circuit and the RF choke in this section. The IF matching transformers design is explained in Section III and we study the heterodyne performance of the complete mixer design predicted by the SuperMix[10] in Section IV. The design of the mixer block and its feed horn is presented in the subsequent section, before we conclude our paper.

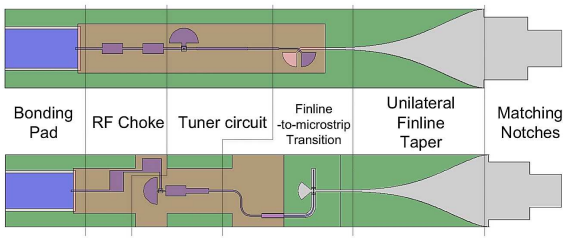


Fig. 2. Overview of the unilateral finline mixer design, with two different types of finline-to-microstrip transition, showing the different components that make up the complete mixer chip.

TABLE I
GENERAL MATERIAL AND DIMENSION OF OUR SIS MIXER CHIPS.

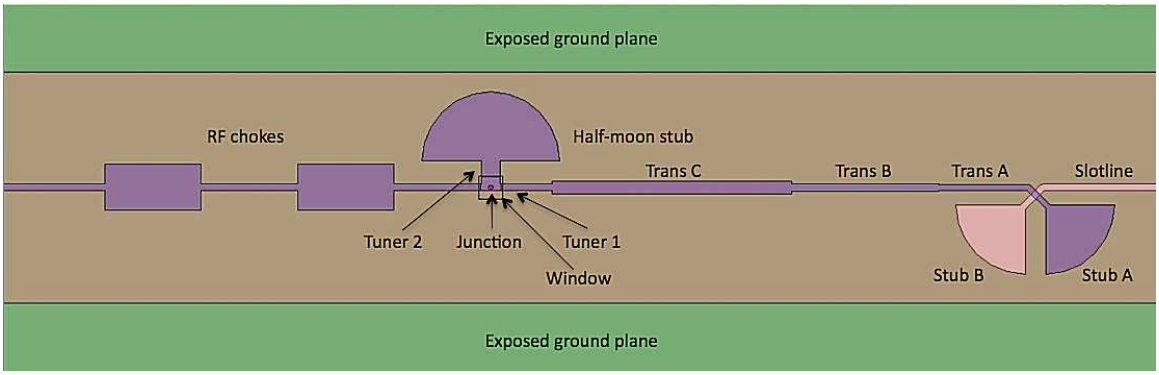
Structure	Material	Dimension
SIS junction	Nb/AlO$_x$/Nb	1 μm^2
Substrate	Silicon	15 μm
Ground plane	Niobium	250 nm
Dielectric layer	Silicon monoxide	475 nm
Signal layer	Niobium	400 nm
Waveguide	Aluminium	320 × 160 μm

II. MIXER DESIGNS

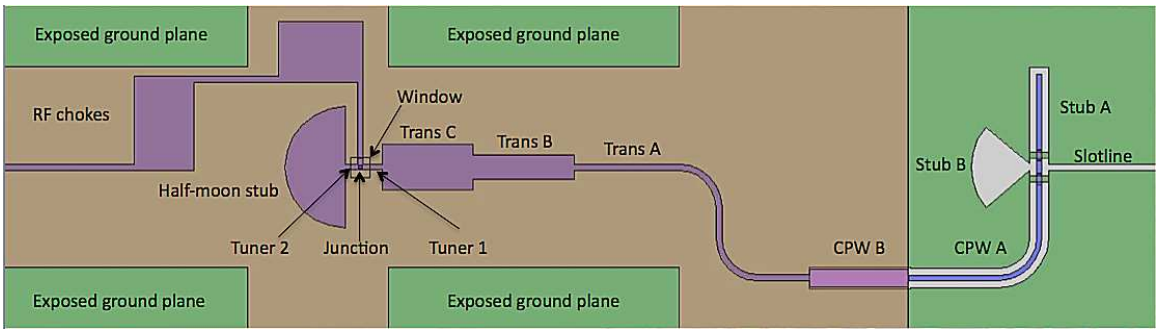
Figure 2 shows the basic components that make up our finline mixer chip. It comprises 6 major sections, following the direction of the RF signal propagation: a 2-step matching notch, unilateral finline taper, finline-to-microstrip transition, superconducting tuning circuit, RF chokes and an IF bonding pad. We have designed two different mixer layouts, differing mainly by the way used to couple power from the finline to the microstrip. The first design employ a direct slotline-to-microstrip transition (herein after known as the direct-mixer) and the second utilize an intermittent coplanar waveguide (CPW) section to better match the impedance of the slotline and the microstrip (herein after known as the CPW-mixer). Our mixers are designed to work in conjunction with a circular Nb/AlO$_x$/Nb SIS tunnel junction with the total area of 1 μm^2. This corresponds to a normal resistance of approximately 20 Ω and junction capacitance of 75 fF, leading to $\omega R_n C \simeq 1$ at 650 GHz. Table I summarizes the material and dimensions of the common structures used in both mixer designs.

The mixer design procedure is rather straightforward, using various commercially or freely available software packages, and is summarized as follow:

1) Finline taper designed using FinSynth [7] or HFSS.
2) Transition from finline to microstrip, mixer tuning circuit, IF choke and other superconducting circuits using Ansoft Designer and HFSS.
3) Superconductivity was included by inserting surface inductance to the perfect conductor structure in HFSS
4) Complete mixer chip simulation in HFSS.
5) Mixer performances verified using SuperMix by feeding the scattering matrices of electromagnetic components from HFSS.



(a) Direct fineline-to-microstrip transition



(b) Transition via coplanar waveguide

Fig. 3. Two different types of unilateral finline SIS mixer employing SOI substrate.

A. *Finline-to-microstrip transition*

Complex superconducting planar circuits are usually fabricated in microstrip because this type of transmission line confines the frequency independent TEM fields between the strip and the ground plane well. Once the RF power is converted into the microstrip mode, the back of the finline chip need not be surrounded by waveguide anymore, hence all additional circuitry can be elegantly incorporated. The transition from the slotline at the output of the unilateral finline to the microstrip can be realized either through direct coupling across the dielectric layer, or more efficiently via intermittent CPW sections. We have designed our mixers using both types of transition. The advantage of the latter option is that it offers a wide range of impedance that can be matched to the relatively high impedance of the unilateral finline. The drawback is that this design is slightly more complicated. Both designs share the same tuning circuit and utilize similar fabrication steps, and can be fabricated on a single wafer. Figure 3 shows the design of the planar circuit for both mixer chips in detail, and the critical dimensions are tabulated in Table II and III. The ”exposed ground plane” in the figure is where the gold beam leads will be deposited to earth the chip. The oxide layer around the junction, about $10 \times 10\mu$m in area, is deposited with only about half of the thickness of the rest of the area. This is to ensure the wiring layer had a good contact with upper layer of the SIS junction.

1) Direct finline-to-microstrip transition (3a): This layout is simple and elegant, however the flexibility in design is much restricted by the lateral dimensional limitation of photolithography in fabricating the slotline and microstrip. The narrowest slotline feasible with modern photolithography is about 2.5 μm, which is about 70 Ω on a 15 μm silicon substrate. This is much higher than the smallest microstrip feasible, i.e. 3 μm wide microstrip is only about 20 Ω. Hence, this mismatch must be included in the design of the transformer section leading to the junction. The incoming slotline is terminated by a 90° radial stub of approximately $\lambda_g/4$ in radius, forcing the RF power to couple to the microstrip. The microstrip line is also terminated by a similar radial stub to provide a short to the incoming RF signal. The advantage of this simple structure is that the RF path is aligned along with the central axis of the mixer chip, and different layers of material are clearly separated, easing the fabrication process.

2) Transition via coplanar waveguide (3b): The impedance of a CPW can be easily adjusted to match that of the slotline and microstrip, since the characteristic impedance of a CPW is largely dependant on the ratio between the width of the central strip and the width of the gaps. The central strip and the ground plane can be fabricated simultaneously in one photolithography step to ensure better symmetrical alignment. We first transform the slotline to a CPW via an extended CPW stub and a radial slotline stub. Two air-bridges are deployed at both side of the slotline, across the CPW, to make sure that the ground planes are equipotential. One slight complication in this design compared to the previous one is that to achieve a low impedance CPW without a very wide central strip, the gap width has to be very small. This ultra-narrow gap can be achieved with a quasi-CPW structure (Section CPW B shown in Figure 3(b)), where the central strip and the ground plane are separated by the thin oxide layer. The gap is defined by

TABLE II
CRITICAL DIMENSION OF THE TUNING CIRCUITS, INCLUDING THE FINLINE-TO-MICROSTRIP TRANSITION, FOR DIRECT TRANSITION MIXER DESIGN. ALL DIMENSION IN μM.

	Stub A	Stub B	Halfmoon Stub	Slotline	Trans A	Trans B	Trans C	Tuner 1	Tuner 2	RF Chokes
Width/Radius	30	30	30	3.0	2.5	3.5	5.5	3.0	8.5	20/3
Length/Angle	90°	90°	180°	50.0	38.5	64.0	104.5	26.5	11.5	42.0

TABLE III
CRITICAL DIMENSION OF THE TUNING CIRCUITS, INCLUDING THE FINLINE-TO-MICROSTRIP TRANSITION, FOR CPW-MIXER DESIGN. ALL DIMENSION IN μM.

	Stub A	Stub B	Halfmoon Stub	Slotline	CPW A	CPW B	Trans A	Trans B	Trans C	Tuner 1	Tuner 2	RF Chokes
Width/Radius	2.5	31.0	30.0	3.0	2.5	8.5	3.0	12.0	23.0	2.5	2.5	30/3
Length/Angle	48.0	80°	180°	60.0	111.5	49.0	155.0	50.0	45.0	10.0	7.0	42.0
CPW gap width	3.5				3.5	1.0						

the effective distance between the edge of the central strip to the ground. Since the central strip and the ground plane of this quasi-CPW section is deposited using two different steps of photolithography, this avoids the problem of short being caused by the ultra-narrow gap. One disadvantage of this structure is that it might cause misalignment of the central strip that leads to imbalanced CPW.

B. Tuner circuit

Conventionally, the tuning circuit used to tuned out the junction capacitance is narrow band, determined primarily by the $\omega R_n C$ constant. The standard method is simply to utilize an inductive strip with an end-stub [8] to tune out the capacitance at a particular frequency. Utilizing the twin-junction method [9] with a microstrip to transform the complex impedance of one junction to the complex conjugate of the other one, can provide a broader band performance, but often with the difficulty that both junctions to be fabricated identically. In the following section, we explain in detail our tuner circuit design methodology which can provide a broad band performance by using only a planar circuit structure with a single SIS junction.

Our tuner circuit is composed of mainly four parts: an inductive strip with a half-moon stub, an inductive strip before the junction, a multi-sections transformer and an RF choke. The dimensions of the various components are tabulated in Table II and III.

In order to match the junction impedance across a broader bandwidth, we make use of two inductive strips, tuned at slightly different frequencies, to provide two poles in the matching circuit. The first utilizes a short microstrip section terminated with a half-moon stub acting as a short. Assuming the load impedance of the half-moon stub is close to zero, the length and the width of this inductive strip can be calculated using the standard transmission line equation simplified to

$$l = \frac{1}{Z_0 \beta \omega C}, \tag{1}$$

where Z_0 is the characteristic impedance of the microstrip line, determining the width of the line, and l is the length of the microstrip line in electrical wavelength, which can be easily converted to actual dimension.

The second pole in the matching circuit make use of another short microstrip line before the junction to tune out the residual impedance at a slightly different frequency (most of the junction impedance had been tuned out by the first inductive strip). Again, the length and width of this microstrip line can be calculated using the standard transmission line equation.

$$Y_s = \frac{Y_l + iY_0 \tan \beta l}{Y_0 + iY_l \tan \beta l} \tag{2}$$

where Y_s is the source impedance, Y_l is the load impedance, which is the residue impedance at the tuned frequency, Y_0 is the characteristic impedance of the line and βl is the propagation constant. By enforcing the imaginary part of Y_s to zero, the length of the strip can thus be obtained in terms of βl. The value of Y_0 can be chosen arbitrarily to determine the width of the line. Combining both inductive strips in conjunction with the junction, the reactance is tuned to zero twice, giving the two poles for better matching.

At this stage, a 3-step transformer is deployed to match the final load impedance (consist of the junction and the two inductive strips) to the input impedance of the slotline. The initial dimension of the transformer can be estimated by standard quarter-wavelength steps, or of Chebyshev design. The transformer matches the Z_0 of the slotline to the real part of the load impedance at the central frequency. The final dimension of transformer can be optimized using conventional software package like HFSS to include various other effects such as the superconducting surface impedance etc.

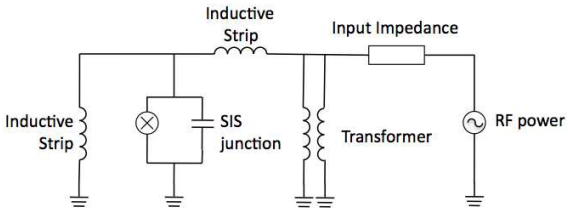
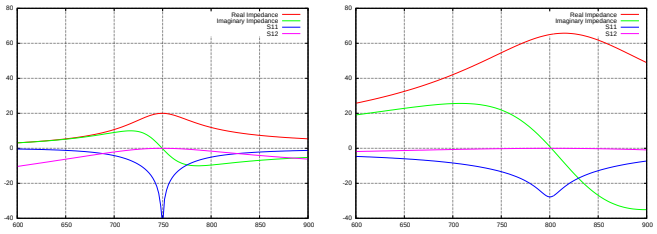
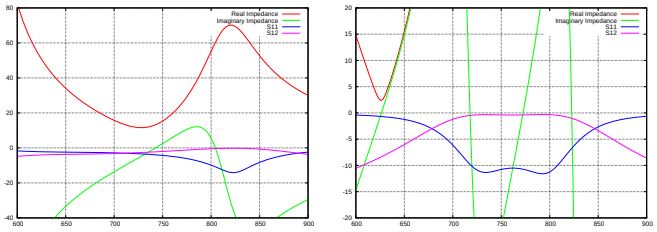


Fig. 4. Electrical diagram of the RF tuning network for our finline mixers.

Figure 4 shows the electrical network representation of our tuning circuit, and Figure 5 illustrates an example using the above method. Figure 5(a) shows the result of using an inductive strip with the half-moon stub to tune out the capacitance of the junction at the first frequency (i.e. 750 GHz in this case). Figure 5(b) shows the result of tuning using the



(a) Inductive strip with half-moon stub (b) Inductive strip before the junction



(c) Combine both inductive strips (d) All tuning components including the transformer

Fig. 5. Example illustrates how each component in the tuning circuits works toward a broadband performance.

second inductive strip to tune out the residual impedance at slightly higher frequency (800 GHz in this case). As can be seen in Figure 5(c), when both the inductive strips are used, there are two poles in the reactance curve that cross the zero axis at the two tuned-out frequencies. Figure 5(d) shows the wide band performance of the tuner after matching the real part of the load impedance to the slotline using the transformer, which exhibit a twin-peaks feature. In this example, the tuning band is tuned slightly higher, as the superconducting surface impedance tends to shift the tuned frequency band downward. It should be noted that this simple circuit representation only gives a preliminarily estimation of the required dimension of various parts. The final design is often simulated and optimised in a 3-D electromagnetic simulators such as HFSS to include effects of thickness, superconducting surface reactance, dielectric tangential loss, etc.

C. RF choke

The RF choke is made of alternating high and low impedance $\lambda_g/4$ sections of microstrip to provide high rejection to the RF signal over the operating band. This avoids RF signal leaking into the IF path and ensure that most of the RF power is coupled to the SIS junction. The width of the high and low impedance sections are chosen so as not to be too narrow or so wide to induce high IF capacitance. We combine all these components into planar circuit together with the unilateral finlines and SOI substrate to simulate the electromagnetic behaviour of the complete mixer chip. Figure 6 shows the return loss and the insertion loss of the complete RF design predicted by HFSS. Both designs have about 100 GHz bandwidth across 600 GHz to 700 GHz band. The power coupled to the junction is better than -0.5 dB in both case, across the operating bandwidth. Outside the design band, the performance of the CPW-mixer deteriorates more slowly compare to the direct-mixer. This is mostly due to the

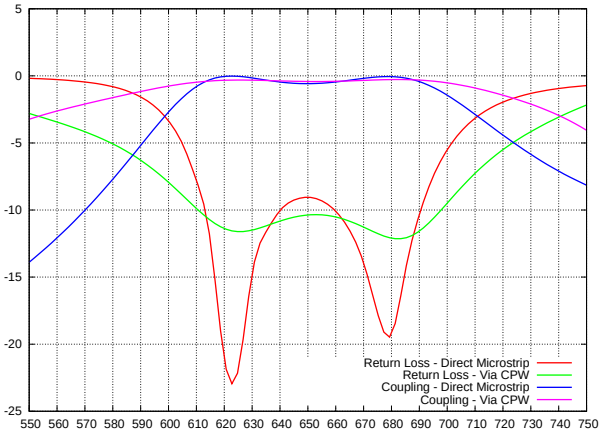


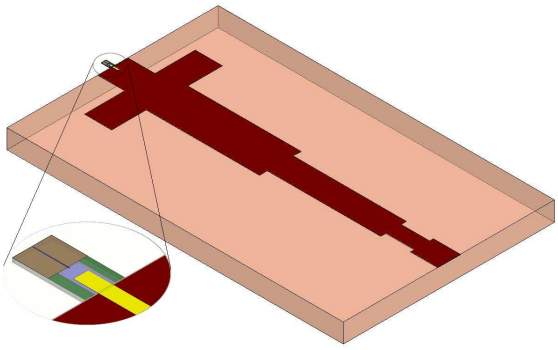
Fig. 6. HFSS simulation shows that the tuner design exhibit broad bandwidth, with about 100 GHz centered at 650 GHz.

severe mismatch of the slotline to microstrip away from the central frequency band.

III. IF TRANSFORMER DESIGN

The physical structure of planar circuits and the finline of the mixer chip will be seen as a lumped RLC load at the IF band, which is not purely resistive. We thus represent the output impedance of the mixer chip as an RLC circuit, and match this load to the 50 Ω input impedance of the low-noise amplifier (LNA), to provide wide IF bandwidth operation. Given that the physical dimensions of both of the mixer designs are similar, the IF impedance would not be very much different, and hence only one IF transformer design is explored. The design procedure are fairly simple, with standard transformer design methodology, and can be optimized using conventional circuit design packages. We use HFSS to provide the flexibility to include more realistic structures such as the bonding pad and the gold beam leads. This is to make certain that we include the effective inductance induced by these structures in the design of the matching transformer.

(a) Flowchart of IF transformer design.



(b) Diagram of IF transformer.

Fig. 7. IF transformer to match the output complex impedance of the mixer chip to the 50 Ω IF output.

TABLE IV
ALL DIMENSION IN MM. IF TRANSFORMER DIMENSION. THE IF TRANSFORMER WILL BE THE SAME FOR BOTH MIXER DESGIN.

	Sect 1	Sect 2	Sect 3	Sect 4	Sect 5	Sect 6	Pocket size
Width	1.00	3.68	1.38	0.86	0.51	0.76	7.0
Length	0.90	0.90	3.76	3.75	0.94	0.9 0	11.15

Figure 7 shows the various components included in the IF transformer design. The following steps summarize the complete design procedure for the IF transformer after the RF part of the mixer design is complete:

1) Obtain the output impedance of the mixer chip seen from the IF port from Ansoft Designer's circuit or SuperMix package
2) At the frequency where the real part of the impedance is zero, find the reactance and estimate the value of the capacitor or inductor
3) Represent the RF mixer chip as an RLC equivalent
4) Use Designer or any other simple circuit simulation package to design the impedance matching transformer
5) Include the gold beam leads and the bonding pads in HFSS to optimize the transformer design
6) Export the scattering matrix into SuperMix to verify the final full mixer heterodyne IF performance

Table IV lists the dimension of the IF transformer used in our mixer design. As can be seen from Figure 8, HFSS calculated that the return loss to be less than -10 dB from about 2 to 12 GHz. This matches very well with our LNA's bandwidth, and is wide enough for most astronomical requirements.

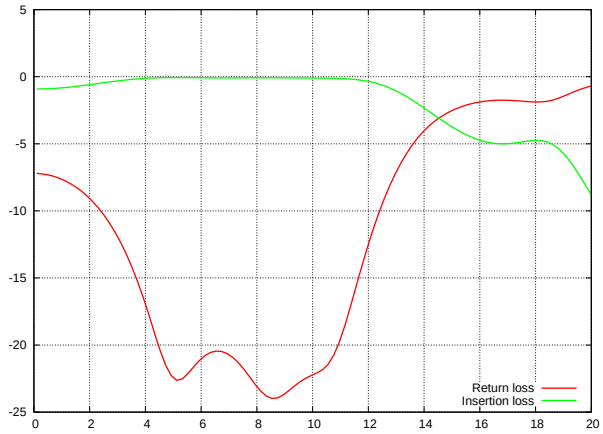


Fig. 8. HFSS simulation shows that the transformer had better than -15 dB return loss from 4 GHz to 12 GHz IF band.

IV. SUPERMIX SIMULATION RESULTS

To verify and understand the heterodyne mixing behaviour of the mixer, we exported the scattering matrices of all the components computed using electromagnetic software package, mainly from HFSS, to SuperMix. In this way, we combine both the more accurate description of electromagnetism behaviour by the electromagnetic package, and make use of SuperMix to predict the superconducting mixer heterodyne performance, such as noise temperature and gain. The dimension obtained from the electromagnetic design can also be input directly to SuperMix as various circuit components for cross-checking purpose, and both methods generally give similar results.

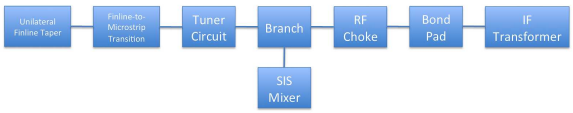


Fig. 9. Flow chart shows the various components included in the SuperMix simulation.

Figure 9 shows all the components included in our SuperMix circuits, and Figure 10 and 11 show the results of the calculation. Both mixer designs yield very flat RF gain response across the operating band. The IF gain is also stable across the desired IF bandwidth. The noise temperature of both mixers is estimated to be lower than 50 K across the whole design band. Again, CPW-mixer design yield a slightly wider RF band, agreeing with the performance predicted by HFSS. These results will serve as a good guideline to better understand the experimental measurement of the real mixer.

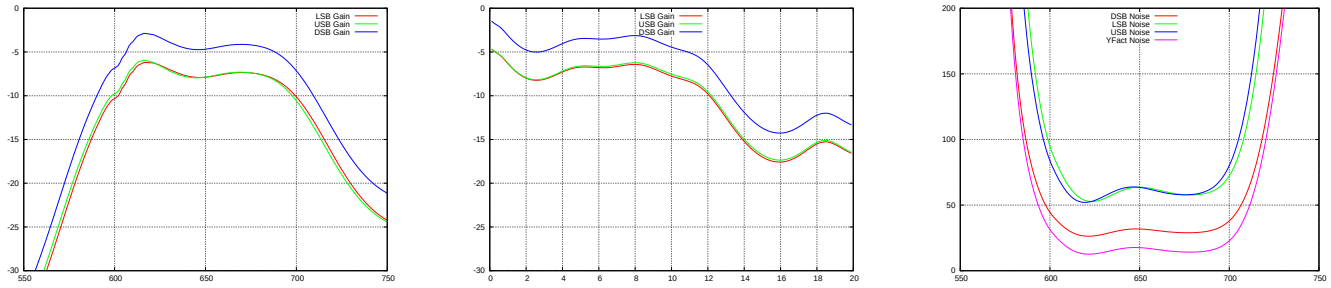
V. MIXER BLOCK AND FEED

The mixer block to house the SOI finline mixer is extremely simple. As shown in Figure 12, only a straight rectangular waveguide is needed, with a pocket for the IF board to be sit on. At the front of the rectangular waveguide is a cone-shaped circular-to-rectangular transition to make sure that the signal from the feed horn is coupled to the mixer chip efficiently. This can be done by simply drilling a 10° opening cone at the inlet of the split-block after the waveguide and other component have been machined. This 10° smooth-cone transition have been demonstrated to work with HARP-B mixers [11] and HFSS simulations predict that the return loss across the band would be less than -20 dB, as shown in Figure 13.

The mixer block will be connected to a smooth-walled horn [12] designed using genetic algorithm. These horns shows good circularity and low side-lobes level, comparable to conventional corrugated horns. They are easy to manufacture and time/cost saving, which is important for multi-pixel focal plane array applications.

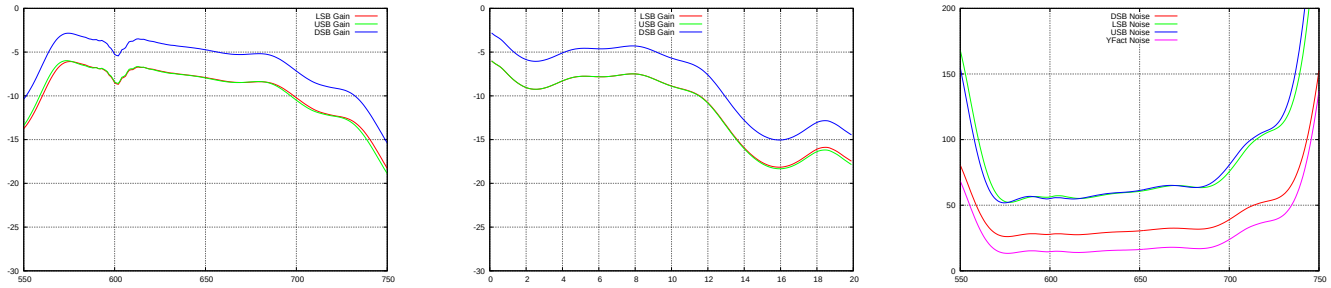
VI. CONCLUSION

We have presented the design of a broadband unilateral finline SIS mixer at 650 GHz utilizing SOI technology. The design results in a tunerless, elegant yet fully integrated planar circuits, and an easy-to-fabricate mixer chip and block. A smooth-walled horn that is manufactured by a simple drilling technique, will be used to feed the signal to the mixer. The use of planar circuit technology ensures that a large number of mixers can be produced in short time and reduces the tolerances between mixer chips. This shall greatly improves the performance and reduces the cost of constructing large-format mixer arrays. The performance was fully simulated using rigourous electromagnetic methods, exported into SuperMix package, and the heterodyne performance has been reported. The chip design will be fabricated at KOSMA, University of Cologne and the experimental measurement of the mixer performance will take place soon.



(a) RF gain (b) IF gain (c) RF noise

Fig. 10. SuperMix simulation results of direct-mixer chip.



(a) RF gain (b) IF gain (c) RF noise

Fig. 11. SuperMix simulation results of CPW-mixer chip.

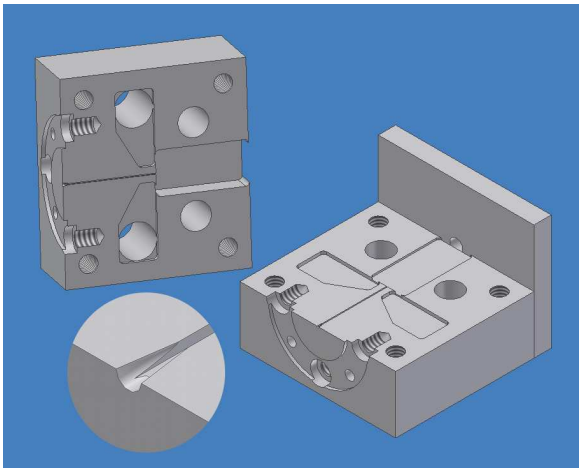


Fig. 12. The drawing of the block that will be used to house the mixer chip. The two butterfly-wing-structure are used to hold the metal that couple the magnetic field from the coil to suppress the Josephson current. It will be fed from the two poles on top of the mixer block. The IF output will be tapped from the IF board using standard SMA connector at the back of the mixer block.

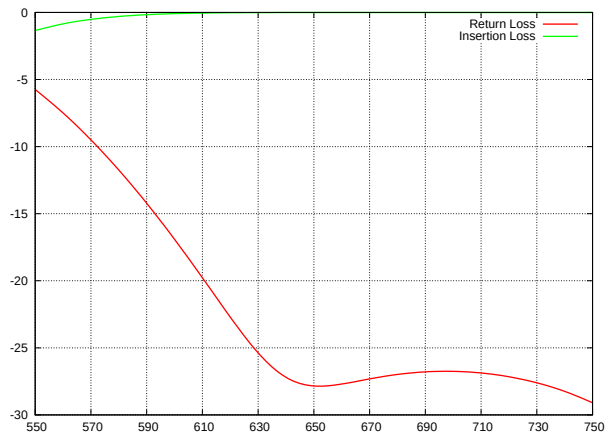


Fig. 13. Return loss and insertion loss for the circular to rectangular waveguide with an opening angle of 10°. The input throat opening of the 700 GHz smooth-walled horn is 408 μm.

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